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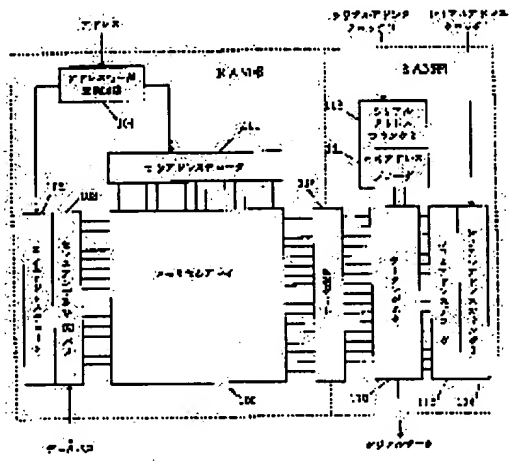
(54) MULTI-PORT MEMORY AND DISPLAY SYSTEM PROVIDED WITH THE SAME

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a multi-port memory whereby rotation display is easily executed and its display system.

SOLUTION: The multi-port memory which transfers data stored in a RAM part to a SAM part by low address unit so as to output data is provided with a low address decoder 111 for designating plural continuous low addresses at every column address and a column address decoder 112 for designating plural continuous column addresses at every low address. The multi-port memory is also the one for outputting data transferred to the SAM part as serial data in a string direction or a row direction.



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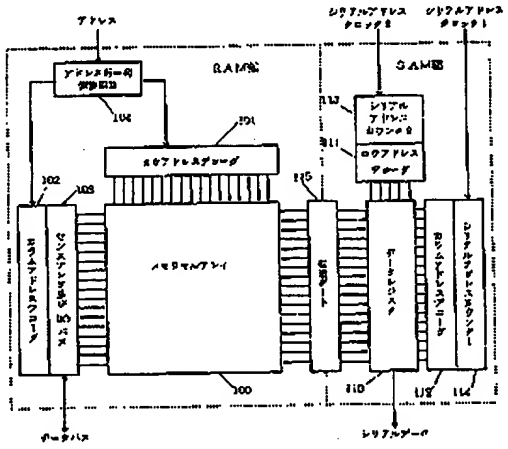
(54)【発明の名称】　マルチポートメモリおよびマルチポートメモリを備えた表示システム

(57)【要約】
【課題】　容易に回転表示を行うことができるマルチポートメモリおよびその表示システムを提供する。
【解決手段】　ＲＡＭ部に記憶されたデータをロウアドレス単位にＳＡＭ部に転送してデータ出力を行うマルチポートメモリにおいて、ＳＡＭ部に、連続した複数のロウアドレスをカラムアドレス毎に指定するロウアドレスレコーダと、連続した複数のカラムアドレスをロウアドレス毎に指定するカラムアドレスレコーダとを設け、ＳＡＭ部に転送されたデータを列方向または行方向のシリアルデータとして出力するマルチポートメモリである。



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【特許請求の範囲】

【請求項１】　ランダムアクセスメモリ部に記憶されたデータをロウアドレス単位にシリアルアクセスメモリ部に転送してデータ出力を行うマルチポートメモリであって．

前記シリアルアクセスメモリ部に連続した複数のロウアドレスをカラムアドレス毎に指定するロウアドレスレコーダと、

連続した複数のカラムアドレスをロウアドレス毎に指定するカラムアドレスレコーダとを設け．

前記シリアルアクセスメモリ部に転送されたデータを列方向または行方向のシリアルデータとして出力することを特徴とするマルチポートメモリ。

【請求項２】　前記ロウアドレスレコーダ及び前記カラムアドレスレコーダは各々アドレスカウンタを備え、

前記ロウアドレスまたはカラムアドレスを、スタートアドレスからインクリメントまたはデクリメントすることにより、任意の順序で前記シリアルアクセスメモリ部に転送されたデータを列方向または行方向のシリアルデータとして出力することを特徴とする請求項１記載のマルチポートメモリ。

【請求項３】　前記ランダムアクセスメモリ部に．ロウアドレスとカラムアドレスを入れ替える行列変換回路を設け．

前記ランダムアクセスメモリ部にデータが書き込まれる際に行列変換を行うことを特徴とする請求項２記載のマルチポートメモリ。

【請求項４】　表示装置と．

前記表示装置に表示するデータを格納する前記マルチポートメモリと．

前記表示装置への画面走査と同期して前記マルチポートメモリのシリアルメモリ部からデータを読み出し．前記表示装置への表示を行う表示制御装置と、

当該表示制御装置を制御する中央処理装置を具備し、

前記中央処理装置は、前記マルチポートメモリのランダムアクセスメモリ部からシリアルアクセスメモリ部への転送を、ランダムアクセスメモリ部のロウアドレスをデクリメントする方向に行わせ、

前記表示制御装置は、前記マルチポートメモリに対し、

前記シリアルアクセスメモリ部の連続した複数のロウアドレスをカラムアドレス毎に指定させる共に、前記スタートアドレスからシリアルアクセスメモリ部のカラムアドレスをデクリメントする方向でアドレス指定させてシリアルデータ出力を行わせ．

前記前記表示装置への画像表示を１８０度回転して行うことを特徴とする請求項１乃至３記載のマルチポートメモリを備えた表示システム。

【請求項５】　前記マルチポートメモリのランダムアクセスメモリ部への書き込み時に前記行列変換を行い、

前記マルチポートメモリのランダムアクセスメモリ部からシリアルアクセスメモリ部への転送を、ランダムアクセスメモリ部のロウアドレスをデクリメントする方向に行い．

前記シリアルアクセスメモリ部の連続した複数のカラムアドレスをロウアドレス毎に指定させ．

前記表示制御装置により．スタートアドレスからシリアルアクセスメモリ部のロウアドレスをデクリメント、カラムアドレスをインクリメントする方向で読み出すことにより、

前記表示装置への表示を２７０度回転した画像を表示することを特徴とする請求項４記載の表示システム。

【請求項６】　前記マルチポートメモリのランダムアクセスメモリ部への書き込み時に前記行列変換を行い、

前記マルチポートメモリのランダムアクセスメモリ部からシリアルアクセスメモリ部への転送を、ランダムアクセスメモリ部のロウアドレスをインクリメントする方向に行い、

前記シリアルアクセスメモリ部の連続した複数のカラムアドレスをロウアドレス毎に指定させ．

前記表示制御装置より、スタートアドレスからシリアルアクセスメモリ部のロウアドレスをインクリメント、カラムアドレスをデクリメントする方向で読み出すことにより．

前記表示装置への表示を９０度回転した画像を表示できることを特徴とする請求項４記載の表示システム。

【請求項７】　ランダムアクセス可能なＲＡＭ部と、

前記ＲＡＭ部のロウアドレスおよびカラムアドレスのそれぞれに対応した２つのシリアルアクセス可能なＳＡＭ部とを備え、

前記ＲＡＭ部のカラムアドレスデータをＲＡＭ部カラムアドレスに対応したＳＡＭ部にデータを格納する際に、データ並びを回転させることを特徴とするマルチポートメモリ。

【請求項８】　表示装置と．

前記表示装置に表示するデータを記憶する前記マルチポートメモリと．

前記表示装置への画面走査と同期して前記マルチポートメモリの前記ＳＡＭ部からデータを読み出し、前記表示装置への表示を行う表示制御装置と．

前記表示制御装置を制御する中央処理装置とを具備し、

前記ＳＡＭ部は．前記ＲＡＭ部から前記ＲＡＭ部のロウアドレス、カラムアドレスに各々対応したデータレジスタを備え、

前記ＲＡＭ部から前記ＲＡＭ部のロウアドレスに対応した前記ＳＡＭ部のデータレジスタにデータの転送を行うことにより、前記表示装置で通常表示および１８０度回転表示を行い．

前記ＲＡＭ部から前記ＲＡＭ部のカラムアドレスに対応した前記ＳＡＭ部のデータレジスタにデータの転送を行うことにより．前記表示装置で９０度および２７０度回

転表示を行うことを特徴とする請求項7記載のマルチポートメモリを備えた表示システム。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明はマルチポートメモリおよびマルチポートメモリを備えた表示システムに関し、特に画像の回転表示に関する。

【0002】

【従来の技術】従来、特開平6－289848号公報には、図13に示すように、表示制御装置800内にVRAM802のアドレスを制御する表示アドレス発生部803を持ち、CPU801から回転表示が指示された場合、表示アドレス発生部803による表示アドレスの生成方法の切り替えと、表示制御部804による表示データのビット順変換によって、VRAM802の内容が180度回転した状態での表示を可能にし、ソフトウェアで書き換える方式に比べ高速の回転表示を実現している。

【0003】また、図14に示すマルチポートRAMは、ランダムアクセス用の4ビットの入出力ポートI/O3～0と、シリアルアクセス用の4ビットの出力ポートSout3～0と、データ記憶用のメモリセルアレイ(512×512×4)900と、このメモリセルアレイ900の行アドレスを生成するロウアドレスデコーダ901と、列アドレスを生成するカラムアドレスデコーダ902と、転送ゲート907を介してメモリセルアレイ900から1ロウ(row)単位でデータを取り込むデータレジスタ908と、そのデータレジスタ908のアドレスを指定するSAM部カラムアドレスデコーダ910と、シリアルアクセスに同期してSAM部カラムアドレスをインクリメントするシリアルアドレスカウンタ911などを備えている。

【0004】メモリセルアレイ900は、512×512ビット構成のセルアレイブロックを4層備えている。このマルチポートRAMにおいて、メモリセルアレイ(512×512×4)900に対するシリアルアクセスは、次のように行われる。

【0005】まず、9ビットの行アドレスがロウアドレスバッファ904に送られロウデコーダ901に供給される。そして、メモリセルアレイ(512×512×4)900の4層のセルアレイ層における選択された行線上のメモリセルのデータ(512×4)は、4層構成の転送ゲート907を介してSAMの記憶部であるデータレジスタ908に格納される。

【0006】データレジスタ908に格納されたデータは、SAMカラムアドレスデコーダ910によって4ビット分選択され、その選択された4ビットはシリアルクロック信号SCに同期してシリアル出力バッファ912を介してシリアル出力ポートSout3～0に出力される。このとき、シリアルアドレスカウンタ911はインクリメントされ、SAMカラムアドレスデコーダ911は次アドレスの4ビットデータ選択する。この動作により、データレジスタ908のデータを追続して読み出すことを可能にしている。

【0007】

【発明が解決しようとする課題】これら従来技術のマルチポートメモリでは、RAM部のロウアドレス上のデータをSAM部のデータレジスタに転送し、表示制御部からのシリアルアクセスにより一方向の順番でデータを読み出すため、通常の表示は高速で行えるが回転表示を行うには、CPUによりRAM部にデータが書き込まれる時に回転された状態のデータが書き込まれなければならず、ソフトウェアでこの処理を行うには負荷が大きい。また、特開平6－289848号公報が示すように外部の表示制御装置内のアドレス発生部および表示制御部のみで回転表示を行う場合、180度回転は容易にできても90度、270度の回転表示は困難である。

【0008】そこで本発明は以上の問題点を改善し、容易に回転表示を行うことができるマルチポートメモリおよびその表示システムを提供することを目的とする。

【0009】

【課題を解決するための手段】本発明の請求項1によれば、ランダムアクセス可能なRAM部に、ロウアドレスを指定するロウアドレスデコーダと、カラムアドレスを指定するカラムアドレスデコーダと、データを格納するメモリセルアレイを備え、シリアルアクセス可能なSAM部に、前記RAM部に記憶されたデータを前記RAM部のロウアドレス単位で格納するデータレジスタと、前記RAM部のメモリセルアレイから前期SAM部のデータレジスタにデータを転送する転送ゲートと、前記データレジスタのアドレスを指定するSAM部ロウアドレスデコーダおよびSAM部カラムアドレスデコーダと、SAM部のロウアドレスおよびカラムアドレスをクロック信号によりインクリメントする2つのシリアルアドレスカウンタを備え、SAM部データレジスタのアドレス指定を追続した複数行および1列、もしくは1行および連続した複数列で行うことにより、SAM部データレジスタのデータを列方向もしくは行方向にシリアルアクセスできる構成により上記課題を解決する。

【0010】請求項2によれば、請求項1のマルチポートメモリにおいて、SAM部ロウアドレスカウンタおよびSAM部カラムアドレスカウンタにカウント値を指定されたスタートアドレスからインクリメントおよびデクリメントできる機能を備え、SAM部データレジスタのデータを任意の順番で読み出す構成により上記課題を解決する。

【0011】請求項3によれば、請求項1および請求項2の構成を持つマルチポートメモリにおいて、ランダムアクセス可能なRAM部にロウアドレスおよびカラムアドレスを入れ替える回路(アドレス行一列変換回路)を備え、書き込まれるデータの配置を行一列において入れ替えることを可能にする構成により上記課題を解決する。

【００１２】請求項４によれば、表示装置と、この表示装置に表示するデータを格納する請求項３のマルチポートメモリと、前記表示装置への画面走査と同期して前記マルチポートメモリのＳＡＭ部からデータを読み出し、前記表示装置への表示を行う表示制御装置と、この表示制御装置を制御する中央処理装置を具備し、前記マルチポートメモリのＲＡＭ部からＳＡＭ部への転送をＲＡＭ部ロウアドレスをデクリメントする方向に行い．ＳＡＭ部データレジスタのアドレス指定を連続した複数行のＳＡＭ部ロウアドレスと１列のＳＡＭ部カラムアドレスで行い．前記表示制御装置より２つのシリアルアクセスクロックを用いて．スタートアドレスからＳＡＭ部カラムアドレスをデクリメントする方向でデータをシリアルアクセス方式で読み出すことにより、前記表示装置への画像表示を１８０度回転して行うことを可能にする構成により上記課題を解決する。

【００１３】請求項５によれば、請求項４の表示システムにおいて、請求項３のマルチポートメモリのＲＡＭ部へのデータ書き込みの際に．ＲＡＭ部ロウアドレスとＲＡＭ部カラムアドレスの入れ替えを前記ＲＡＭ部のアドレス行一列変換回路で行い．前記マルチポートメモリのＲＡＭ部からＳＡＭ部への転送をＲＡＭ部ロウアドレスをデクリメントする方向に行い、ＳＡＭ部データレジスタのアドレス指定を１行のＳＡＭ部ロウアドレスと連続した複数列のＳＡＭ部カラムアドレスで行い、表示制御装置より２つのシリアルアクセスクロックを用いて、スタートアドレスからＳＡＭ部ロウアドレスをデクリメント．ＳＡＭ部カラムアドレスをインクリメントする方向でデータをシリアルアクセス方式で読み出すことにより．前記表示装置への画像表示を時計回りに２７０度回転して行うことを可能にする構成により上記課題を解決する。

【００１４】請求項６によれば、請求項４の表示システムにおいて、請求項３のマルチポートメモリのＲＡＭ部へのデータ書き込みの際に．ＲＡＭ部ロウアドレスとＲＡＭ部カラムアドレスの入れ替えを前記ＲＡＭ部のアドレス行一列変換回路で行い．前記マルチポートメモリのＲＡＭ部からＳＡＭ部への転送をＲＡＭ部ロウアドレスをインクリメントする方向に行い、ＳＡＭ部データレジスタのアドレス指定を１行のＳＡＭ部ロウアドレスと連続した複数列のＳＡＭ部カラムアドレスで行い．表示制御装置より２つのシリアルアクセスクロックを用いて、スタートアドレスからＳＡＭ部ロウアドレスをインクリメント、ＳＡＭ部カラムアドレスをデクリメントする方向でデータをシリアルアクセス方式で読み出すことにより．前記表示装置への画像表示を時計回りに９０度回転して行うことを可能にする構成により上記課題を解決する。

【００１５】請求項７によれば、ランダムアクセス可能なＲＡＭ部に．ロウアドレスを指定するロウアドレスデコーダと、カラムアドレスを指定するカラムアドレスデコーダと、データを格納するメモリセルアレイを備え、シリアルアクセス可能なＳＡＭ部に．前期ＲＡＭ部に記憶されたデータを前期ＲＡＭ部のロウアドレス単位で格納する第１のデータレジスタと、前期ＲＡＭ部に記憶されたデータを前期ＲＡＭ部のカラムアドレス単位で格納する第２のデータレジスタと、前期ＲＡＭ部のメモリセルアレイから前期ＳＡＭ部のデータレジスタにデータを転送する転送ゲートと、前期データレジスタのアドレスを指定するアドレスデコーダと、アドレスをシリアルアクセスクロックによってカウントするシリアルアドレスカウンタと、２つのデータレジスタの選択を切り替えるデータレジスタ選択回路とを備え、ＲＡＭ部のカラムアドレスが指すメモリセルの並びと、第２のデータレジスタの並びを変更することにより、容易に回転表示のできる構成により上記課題を解決する。

【００１６】請求項８によれば、表示装置と、この表示装置に表示するデータを格納する請求項７のマルチポートメモリと、前記表示装置への画面走査と同期して前記マルチポートメモリのＳＡＭ部からデータを読み出し、前記表示装置への表示を行う表示制御装置と、この表示制御装置を制御する中央処理装置を具備し、前期マルチポートメモリのデータレジスタ選択回路でＲＡＭ部ロウアドレスに対応した第１のＳＡＭ部データレジスタを選択することにより、前期表示制御装置からのシリアルアクセスクロックで、シリアルアドレスカウンタのインクリメントおよびデクリメントを行うことで、画像の通常表示および１８０度回転表示を行い．前期データレジスタ選択回路でＲＡＭ部カラムアドレスに対応した第２のＳＡＭ部データレジスタを選択することにより．前期表示制御装置からのシリアルアクセスクロックで．シリアルアドレスカウンタのインクリメントおよびデクリメントを行うことで．時計回りに９０度および２７０度回転した画像表示を行うことを可能にする構成により上記課題を解決する。

【００１７】

【発明の実施の形態】以下に、本発明の実施例について図を参照しながら説明する。図１は第１、第２．第３の発明のマルチポートメモリのブロック図である。図２は図１のマルチポートを使用した表示システムのブロック図である。図５．図６、図７、図８はそれぞれ図２の表示システムで回転表示が行われるときのマルチポートメモリのデータ配置とＬＣＤの表示状態を示しており、ここでは説明を容易にするため８×８×２のマルチポートメモリおよび８×８のＬＣＤを用いている。ＬＣＤは図の左上から右下に向かって順に走査される。

【００１８】図１において．100は表示データを格納するメモリセルアレイ、101はＲＡＭ部ロウアドレスデコーダ．102はＲＡＭ部カラムアドレスデコーダである。103はセンスアンプおよびI/Oバスで、システムのデータ

バスと接続される。104はアドレス行一列変換回路で、時計回りに９０度および２７０度の回転表示が指示されると、ＲＡＭ部のロウアドレスとカラムアドレスを入れ替える。115は転送ゲートで、ＲＡＭ部のメモリセルアレイ100からロウアドレスデコーダ101で指示されるデータをＳＡＭ部に転送する。110はデータレジスタで、転送ゲート115により転送される表示データが格納され、シリアルアクセスによってデータを出力する。111はＳＡＭ部ロウアドレスデコーダ、112はＳＡＭ部カラムアドレスデコーダで、同時に連続した複数行および複数列のアドレス指示を行うことができる。113はＳＡＭ部ロウアドレスのためのシリアルアドレスカウンタ、114はＳＡＭ部カラムアドレスのためのシリアルアドレスカウンタであり、それぞれスタートアドレスからのインクリメントおよびデクリメントができる。

【００１９】図２において、200は中央処理装置、201は表示制御装置、202はＬＣＤ、203は図１のマルチポートメモリであり、２つのシリアルアドレスクロック入力を持っている。

【００２０】図２の表示システムにおいて、画像を通常の状態で表示するとき、図５のメモリのデータ配置になる。アドレス行一列変換回路104は機能せず、メモリセルアレイ100には図５に示すようにデータが格納される。データレジスタ110にはＲＡＭ部ロウアドレスＲ０からＲ７の順番でデータが転送される。ＳＡＭ部ロウアドレスデコーダ111が２行のアドレスｒ０、ｒ１を絶えず指示し、ＳＡＭ部カラムアドレスデコーダ112が１列のアドレスをｃ０からｃ３の順番で指示することにより、データレジスタ110に転送されたデータは図１に示すシリアルアドレスクロック１に同期して2-bitづつ出力される。そのデータを表示制御装置201によりＬＣＤ202に順次表示することにより通常の表示が行われる。

【００２１】画像を１８０度回転した状態で表示するとき、図６のメモリのデータ配置になる。アドレス行一列変換回路104は機能せず、メモリセルアレイ100には図８に示すようにデータが格納される。データレジスタ110にはＲＡＭ部ロウアドレスＲ７からＲ０の順番でデータが転送される。ＳＡＭ部ロウアドレスデコーダ111が２行のアドレスｒ０、ｒ１を絶えず指示し、ＳＡＭ部カラムアドレスデコーダ112が１列のアドレスをｃ３からｃ０の順番で指示することで、データレジスタ110に転送されたデータは、図１に示すシリアルアドレスクロック１に同期して2-bitづつ出力される。そのデータを表示制御装置201によりＬＣＤ202に順次表示することにより１８０度回転した画像の表示が行われる。

【００２２】画像を時計回りに２７０度回転した状態で表示するとき、図７のメモリのデータ配置になる。アドレス行一列変換回路104により、ＲＡＭ部ロウアドレスとＲＡＭ部カラムアドレスが入れ替えられ、メモリセルアレイ100には図７に示すようにデータが格納される。データレジスタ110にはＲＡＭ部ロウアドレスＲ３からＲ０の順番でデータが転送される。ＳＡＭ部ロウアドレスデコーダ111が１行のアドレスｒ１を指示し、ＳＡＭ部カラムアドレスデコーダ112が２列のアドレスをｃ０、ｃ１からｃ６，ｃ７の順番で指示することにより、ＳＡＭ部ロウアドレスｒ１が指示するデータが、図１に示すシリアルアドレスクロック１に同期して2-bitづつ出力される。次に、図１に示すシリアルアドレスクロック２を入力することにより、ＳＡＭ部ロウアドレスの指示をｒ０に移し、もう一度、カラムアドレスデコーダ112が２列のアドレスをｃ０，ｃ１からｃ６，ｃ７の順番で指示することにより、ＳＡＭ部ロウアドレスｒ０が指示するデータが、図１に示すシリアルアドレスクロック１に同期して2-bitづつ出力される。そのデータを表示制御装置201によりＬＣＤ202に順次表示することにより時計回りに２７０度回転した画像の表示が行われる。

【００２３】画像を時計回りに９０度回転した状態で表示するとき、図８のメモリのデータ配置になる。アドレス行一列変換回路104により、ＲＡＭ部ロウアドレスとＲＡＭ部カラムアドレスが入れ替えられ、メモリセルアレイ100には図８に示すようにデータが格納される。データレジスタ110にはＲＡＭ部ロウアドレスＲ０からＲ３の順番でデータが転送される。ＳＡＭ部ロウアドレスデコーダ111が１行のアドレスｒ０を指示し、ＳＡＭ部カラムアドレスデコーダ112が２列のアドレスをｃ７、ｃ６からｃ１、ｃ０の順番で指示することにより、ＳＡＭ部ロウアドレスｒ０が指示するデータが、図１に示すシリアルアドレスクロック１に同期して2-bitづつ出力される。次に、図１に示すシリアルアドレスクロック２を入力することにより、ＳＡＭ部ロウアドレスの指示をｒ１に移し、もう一度、カラムアドレスデコーダ112が２列のアドレスをｃ７，ｃ６からｃ１，ｃ０の順番で指示することにより、ＳＡＭ部ロウアドレスｒ１が指示するデータが、図１に示すシリアルアドレスクロック１に同期して2-bitづつ出力される。そのデータを表示制御装置201によりＬＣＤ202に順次表示することにより時計回りに９０度回転した画像の表示が行われる。

【００２４】図３は本発明の他の実施例のマルチポートメモリのブロック図である。図４は図３のマルチポートを使用した表示システムのブロック図である。図９、図１０、図１１、図１２はそれぞれ図４の表示システムで回転表示が行われるときのマルチポートメモリのデータ配置とＬＣＤの表示状態を示しており、ここでは説明を容易にするため８×８×２のマルチポートメモリおよび８×８のＬＣＤを用いている。ＬＣＤは図の左上から右下に向かって順に走査される。

【００２５】図３において、300は表示データを格納するメモリセルアレイ、301はＲＡＭ部ロウアドレスデコーダ、302はＲＡＭ部カラムアドレスデコーダである。303はセンスアンプおよびI/Oバスでシステムのデータバ

スと接続される。315は転送ゲートでＲＡＭ部のメモリセルアレイ300からロウアドレスデコーダ301で指示されるデータをＳＡＭ部に転送する。310はデータレジスタで転送ゲート315により転送される表示データが格納され、シリアルアクセスによってデータを出力する。325も転送ゲートであり、ＲＡＭ部のメモリセルアレイ300からカラムアドレスデコーダ302で指示されるデータをＳＡＭ部に転送する。320はデータレジスタで転送ゲート325により転送される表示データを回転表示が容易に行われるように配置されており、シリアルアクセスによってデータを出力する。312はデータレジスタ310のためのアドレスデコーダ、322はデータレジスタ320のためのアドレスデコーダである。314はＳＡＭ部アドレスデコーダ312および322のためのシリアルアドレスカウンタであり、それぞれスタートアドレスからのインクリメントおよびデクリメントができる。330は２つのデータレジスタ310および320のどちらを使用するか選択するためのデータレジスタ選択回路である。

【００２６】図４において、400は中央処理装置、401は表示制御装置、402はＬＣＤ、403は図３のマルチポートメモリである。図４の表示システムにおいて、画像を通常の状態で表示するとき、図９のメモリのデータ配置になる。メモリセルアレイ300には図９に示すようにデータが格納される。データレジスタ選択回路330により、データレジスタ310が選択され、データレジスタ310にはＲＡＭ部ロウアドレスＲ０からＲ７の順番でデータが転送される。ＳＡＭ部アドレスデコーダ312がアドレスをｃ０からｃ３の順番で指示することにより、データレジスタ310に転送されたデータはシリアルアドレスクロックに同期して2-bitづつ出力される。そのデータを表示制御装置401によりＬＣＤ402に順次表示することにより通常の表示が行われる。

【００２７】画像を１８０度回転した状態で表示するとき、図１０のメモリのデータ配置になる。メモリセルアレイ300には図１０に示すようにデータが格納される。データレジスタ選択回路330により、データレジスタ310が選択され、データレジスタ310にはＲＡＭ部ロウアドレスＲ７からＲ０の順番でデータが転送される。ＳＡＭ部アドレスデコーダ312がアドレスをｃ３からｃ０の順番で指示することにより、データレジスタ310に転送されたデータはシリアルアドレスクロックに同期して2-bitづつ出力される。そのデータを表示制御装置401によりＬＣＤ402に順次表示することにより１８０度回転した画像の表示が行われる。

【００２８】画像を時計回りに２７０度回転した状態で表示するとき、図１１のメモリのデータ配置になる。メモリセルアレイ300には図１１に示すようにデータが格納される。データレジスタ選択回路330により、データレジスタ320が選択され、データレジスタ320にはＲＡＭ部カラムアドレスＣ３からＣ０の順番でデータが転送される。データレジスタ320に転送されたデータは図１１に示すように配置される。ＳＡＭ部アドレスデコーダ322がアドレスをｒ０からｒ７の順番で指示することにより、データレジスタ320に転送されたデータはシリアルアドレスクロックに同期して2-bitづつ出力される。そのデータを表示制御装置401によりＬＣＤ402に順次表示することにより時計回りに２７０度回転した画像の表示が行われる。

【００２９】画像を時計回りに９０度回転した状態で表示するとき、図１２のメモリのデータ配置になる。メモリセルアレイ300には図１２に示すようにデータが格納される。データレジスタ選択回路330により、データレジスタ320が選択され、データレジスタ320にはＲＡＭ部カラムアドレスＣ０からＣ３の順番でデータが転送される。データレジスタ320に転送されたデータは図１２に示すように配置される。ＳＡＭ部アドレスデコーダ322がアドレスをｒ７からｒ０の順番で指示することにより、データレジスタ320に転送されたデータはシリアルアドレスクロックに同期して2-bitづつ出力される。そのデータを表示制御装置401によりＬＣＤ402に順次表示することにより時計回りに９０度回転した画像の表示が行われる。

【００３０】

【発明の効果】請求項１記載のマルチポートメモリによれば、シリアルアクセスメモリ部に、連続した複数のロウアドレスをカラムアドレス毎に指定するロウアドレスレコーダと、連続した複数のカラムアドレスをロウアドレス毎に指定するカラムアドレスレコーダとを設けたので、マルチポートメモリ内で画像の回転処理を行えるため、ソフトウェアでマルチポートメモリの内容を書き換える方式に比べ、高速の回転表示が可能になるという効果がある。

【００３１】請求項２記載のマルチポートメモリによれば、請求項１記載のマルチポートメモリにおいて、前記ロウアドレスまたはカラムアドレスを、スタートアドレスからインクリメントまたはデクリメントするので、任意の順序で前記シリアルアクセスメモリ部に転送されたデータを列方向または行方向のシリアルデータとして出力することができるという効果がある。

【００３２】請求項３記載のマルチポートメモリによれば、請求項２記載のマルチポートメモリにおいて、前記ランダムアクセスメモリ部にデータが書き込まれる際に行列変換を行うので、ランダムアクセスメモリ部にデータが書き込まれる際に自動的に行列変換を行うことができるという効果がある。

【００３３】請求項４乃至請求項６記載の表示システムによれば、請求項１乃至請求項３記載のマルチポートメモリにより、画像を９０度、１８０度、２７０度回転表示する際に、ソフトウェアなどによる回転処理したデータをマルチポートメモリに書き込む必要がなくなり、非

寧に高速な回転表示を実現することができるという効果がある。

【0034】請求項7記載のマルチポートメモリによれば、RAM部のカラムアドレスデータをRAM部カラムアドレスに対応したSAM部にデータを格納する際に、データ並びを回転させるので、回転表示に必要なデータの並びの変更を容易に行うことができるという効果がある。

【0035】請求項8記載のマルチポートメモリによれば、請求項7記載のマルチポートメモリにおいて、前記RAM部から前記RAM部のロウアドレスに対応した前記SAM部のデータレジスタにデータの転送を行うことにより、前記表示装置で通常表示および180度回転表示を行い、前記RAM部から前記RAM部のカラムアドレスに対応した前記SAM部のデータレジスタにデータの転送を行うことにより、前記表示装置で90度および270度回転表示を行うので、ソフトウェアなどによる回転処理したデータをマルチポートメモリに書き込む必要がなくなり、非常に高速な回転表示を実現することができるという効果がある。

【図面の簡単な説明】

【図1】本発明の一実施の形態のマルチポートメモリのブロック図である。

【図2】本発明の一実施の形態表示システムのブロック図である。

【図3】本発明の他の実施の形態のマルチポートメモリのブロック図である。

【図4】本発明の他の実施の形態の表示システムのブロック図である。

【図5】図2の表示システムにおける通常表示時のマルチポートメモリのデータ配置図である。

【図6】図2の表示システムにおける180度回転表示時のマルチポートメモリのデータ配置図である。

【図7】図2の表示システムにおける時計回りに270度回転表示時のマルチポートメモリのデータ配置図である。

【図8】図2の表示システムにおける時計回りに90度回転表示時のマルチポートメモリのデータ配置図である。

【図9】図4の表示システムにおける通常表示時のマルチポートメモリのデータ配置図である。

【図10】図4の表示システムにおける180度回転表示時のマルチポートメモリのデータ配置図である。

【図11】図4の表示システムにおける時計回りに270度回転表示時のマルチポートメモリのデータ配置図である。

【図12】図4の表示システムにおける時計回りに90度回転表示時のマルチポートメモリのデータ配置図である。

【図13】従来技術によるの表示システムのブロック図である。

【図14】従来技術によるマルチポートメモリのブロック図である。

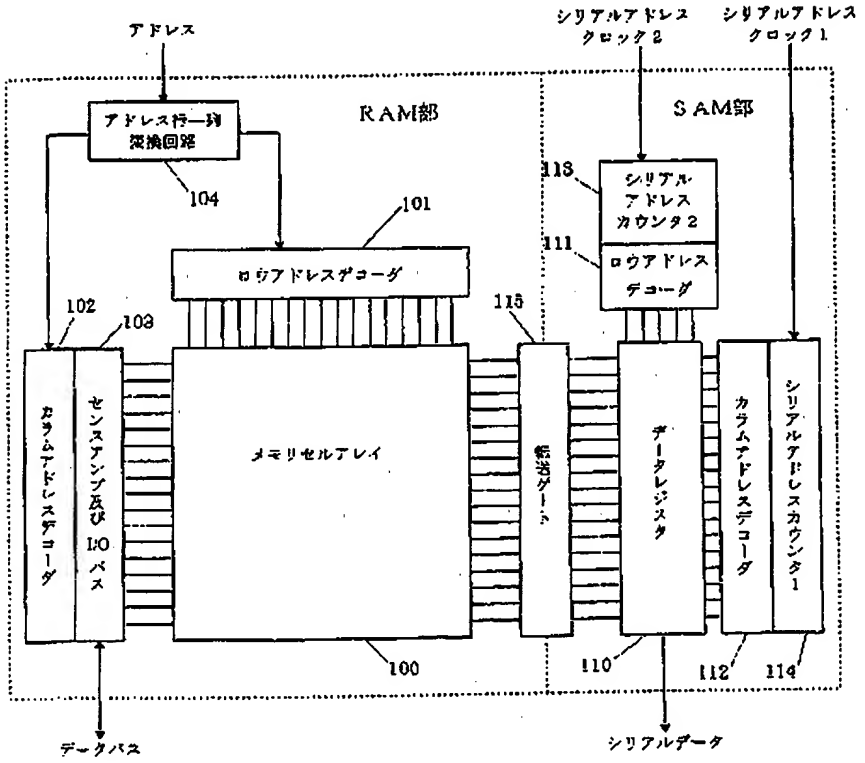
【符号の説明】

100 メモリセルアレイ
101 RAM部ロウアドレスデコーダ
102 RAM部カラムアドレスデコーダ
103 センスアンプおよびI/Oバス
104 アドレス行一列変換回路
110 データレジスタ
111 SAM部ロウアドレスデコーダ
112 SAM部カラムアドレスデコーダ
113 シリアルアドレスカウンタ2
114 シリアルアドレスカウンタ1
115 転送ゲート
200 中央処理装置
201 表示制御装置
202 LCD
203 マルチポートメモリ
300 メモリセルアレイ
301 RAM部ロウアドレスデコーダ
302 RAM部カラムアドレスデコーダ
303 センスアンプおよびI/Oバス
310 データレジスタ1
312 SAM部アドレスデコーダ1
314 シリアルアドレスカウンタ
315 転送ゲート1
320 データレジスタ2
322 SAM部アドレスデコーダ2
325 転送ゲート2
330 データレジスタ選択回路
400 中央処理装置
401 表示制御装置
402 LCD
403 マルチポートメモリ
800 表示制御装置
801 CPU
802 VRAM
803 表示アドレス発生部
804 表示制御部
805 LCD
900 メモリセルアレイ
901 RAM部ロウデコーダ
902 RAM部カラムデコーダ
903 センスアンプおよびI/Oバス
904 ロウアドレスバッファ
905 カラムアドレスバッファ
906 I/Oバッファ
907 転送ゲート
908 データレジスタ

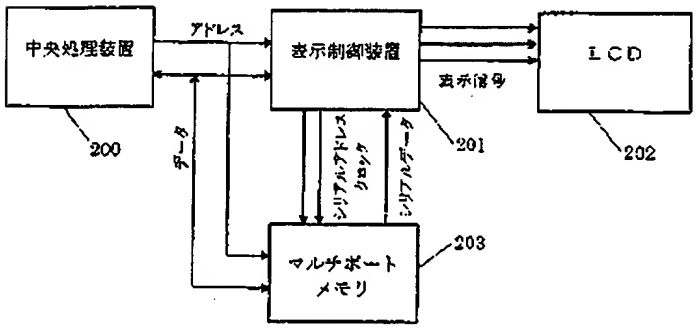
13　　14

909　SAM部出力バス
910　SAM部カラムデコーダ
＊911　シリアルアドレスカウンタ
＊　912　シリアル出力バッファ

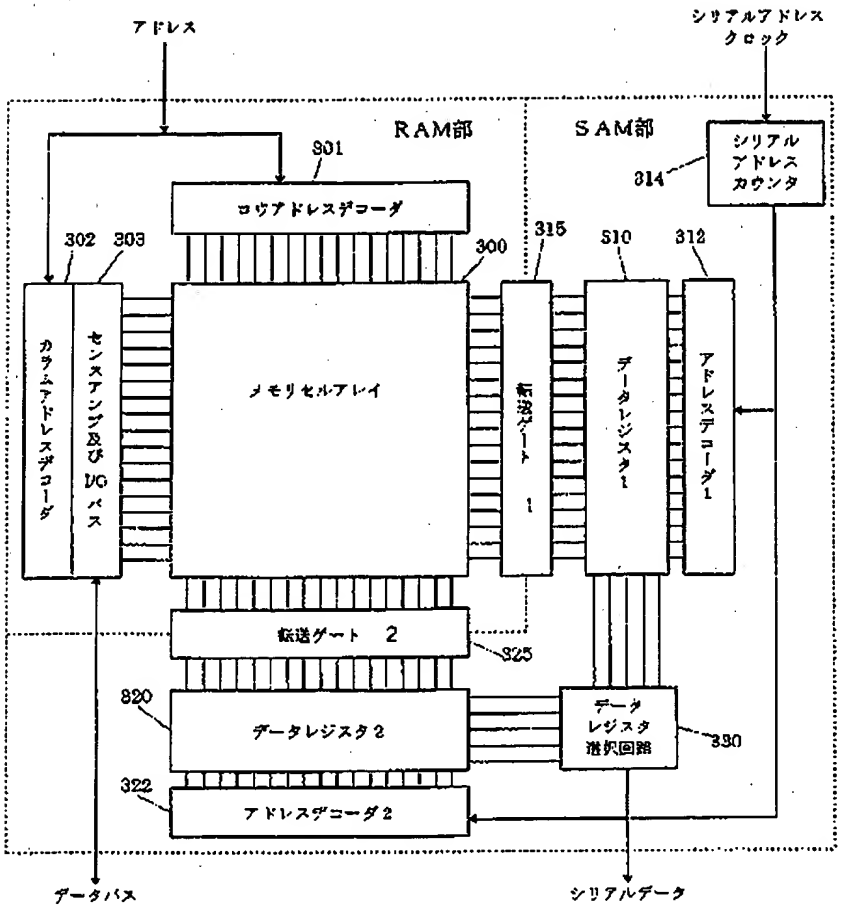
【図1】



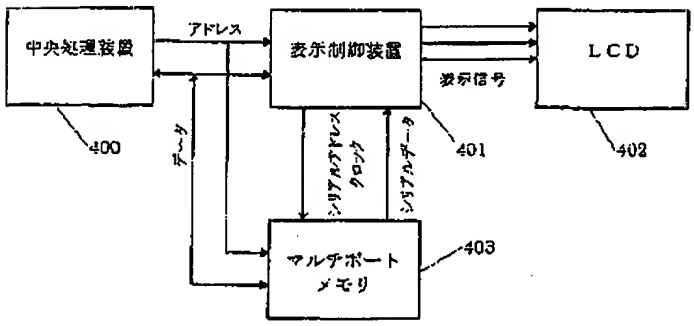
【図2】



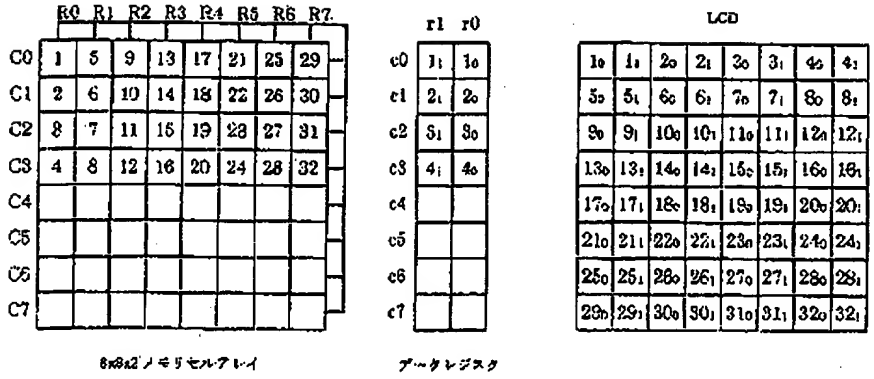
【図3】


アドレス
シリアルアドレス
クロック
RAM部
SAM部
301
ロウアドレスデコーダ
314
シリアル
アドレス
カウンタ
302
303
300
315
310
312
カラムアドレスデコーダ
センスアンプ及び I/O バス
メモリセルアレイ
転送ゲート 1
データレジスタ1
アドレスデコーダ1
転送ゲート 2
325
820
データレジスタ2
データ
レジスタ
選択回路
330
322
アドレスデコーダ2
データバス
シリアルデータ

【図4】

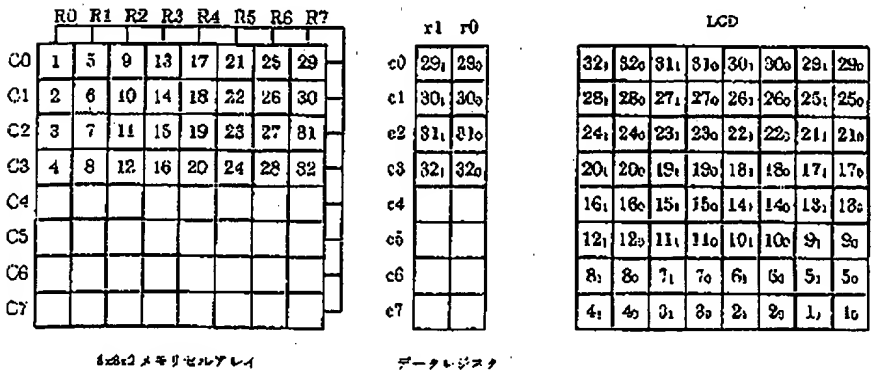

中央処理装置
アドレス
表示制御装置
LCD
表示信号
400
データ
シリアルアドレス
クロック
シリアルデータ
401
402
マルチポート
メモリ
403

【図5】



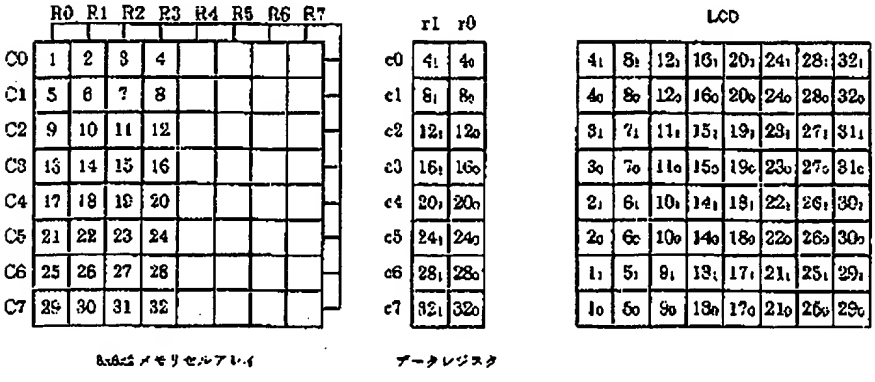
8x8x2メモリセルアレイ　　データレジスタ

【図6】



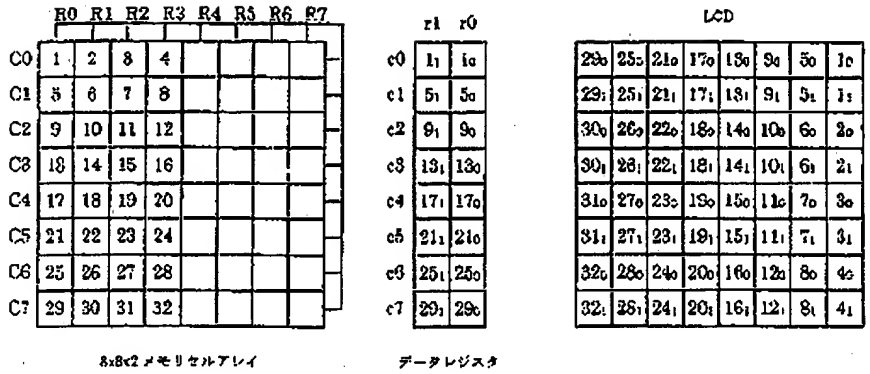
8x8x2メモリセルアレイ　　データレジスタ

【図7】

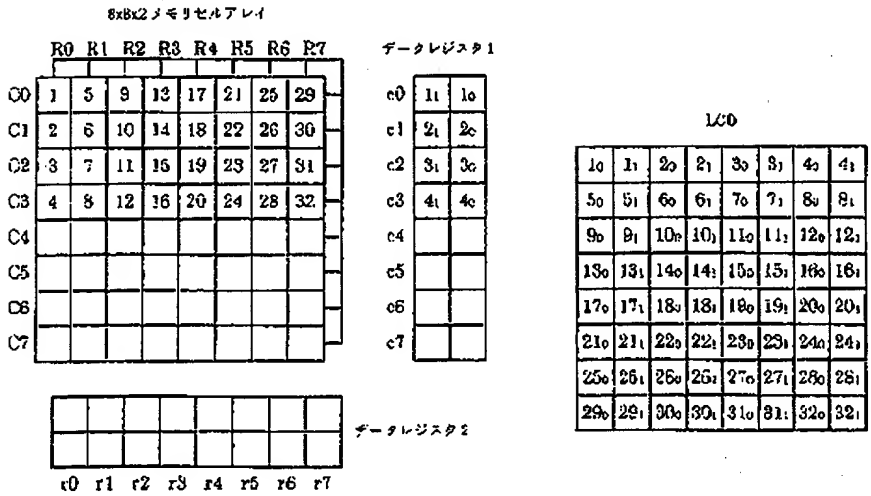


8x8x2メモリセルアレイ　　データレジスタ

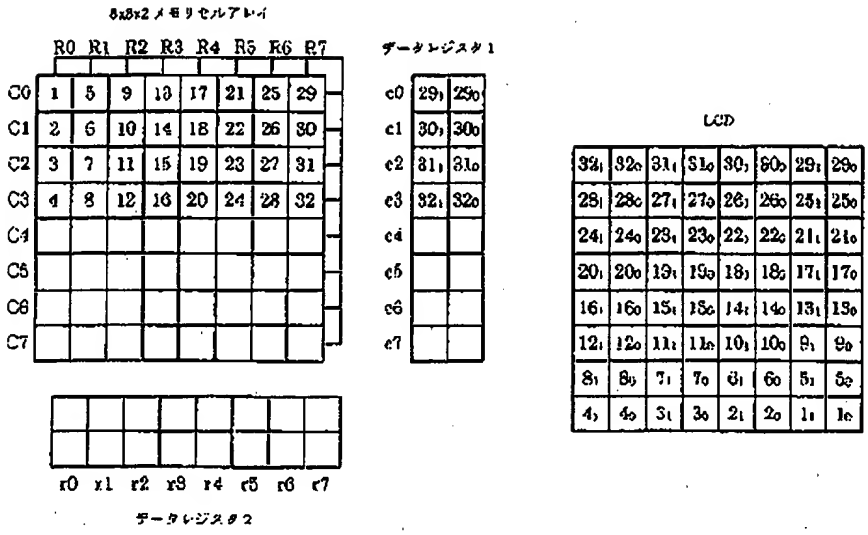
【図8】


R0 R1 R2 R3 R4 R5 R6 R7
C0 1 2 3 4
C1 5 6 7 8
C2 9 10 11 12
C3 13 14 15 16
C4 17 18 19 20
C5 21 22 23 24
C6 25 26 27 28
C7 29 30 31 32
8x8x2メモリセルアレイ
r1 r0
c0 1₁ 1₀
c1 5₁ 5₀
c2 9₁ 9₀
c3 13₁ 13₀
c4 17₁ 17₀
c5 21₁ 21₀
c6 25₁ 25₀
c7 29₁ 29₀
データレジスタ
LCD
29₀ 25₀ 21₀ 17₀ 13₀ 9₀ 5₀ 1₀
29₁ 25₁ 21₁ 17₁ 13₁ 9₁ 5₁ 1₁
30₀ 26₀ 22₀ 18₀ 14₀ 10₀ 6₀ 2₀
30₁ 26₁ 22₁ 18₁ 14₁ 10₁ 6₁ 2₁
31₀ 27₀ 23₀ 19₀ 15₀ 11₀ 7₀ 3₀
31₁ 27₁ 23₁ 19₁ 15₁ 11₁ 7₁ 3₁
32₀ 28₀ 24₀ 20₀ 16₀ 12₀ 8₀ 4₀
32₁ 28₁ 24₁ 20₁ 16₁ 12₁ 8₁ 4₁

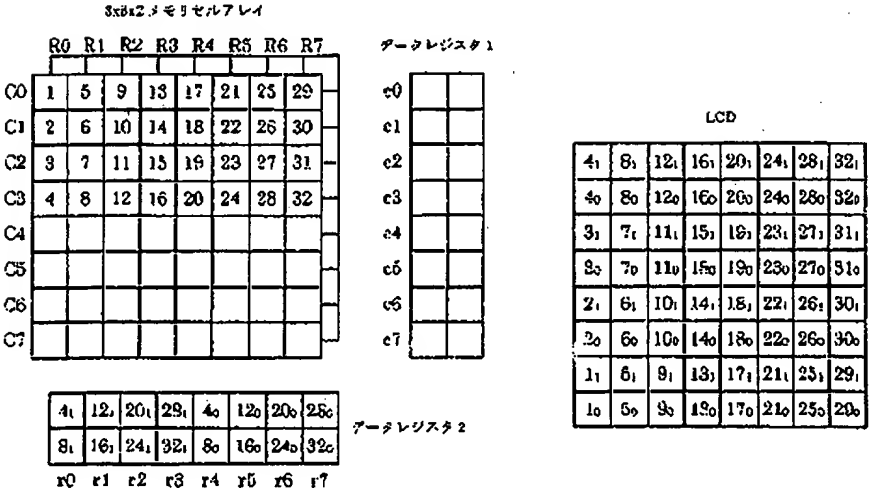
【図9】


8x8x2メモリセルアレイ
R0 R1 R2 R3 R4 R5 R6 R7
C0 1 5 9 13 17 21 25 29
C1 2 6 10 14 18 22 26 30
C2 3 7 11 15 19 23 27 31
C3 4 8 12 16 20 24 28 32
C4
C5
C6
C7
データレジスタ1
c0 1₁ 1₀
c1 2₁ 2₀
c2 3₁ 3₀
c3 4₁ 4₀
c4
c5
c6
c7
データレジスタ2
c0 r1 r2 r3 r4 r5 r6 r7
LCD
1₀ 1₁ 2₀ 2₁ 3₀ 3₁ 4₀ 4₁
5₀ 5₁ 6₀ 6₁ 7₀ 7₁ 8₀ 8₁
9₀ 9₁ 10₀ 10₁ 11₀ 11₁ 12₀ 12₁
13₀ 13₁ 14₀ 14₁ 15₀ 15₁ 16₀ 16₁
17₀ 17₁ 18₀ 18₁ 19₀ 19₁ 20₀ 20₁
21₀ 21₁ 22₀ 22₁ 23₀ 23₁ 24₀ 24₁
25₀ 25₁ 26₀ 26₁ 27₀ 27₁ 28₀ 28₁
29₀ 29₁ 30₀ 30₁ 31₀ 31₁ 32₀ 32₁

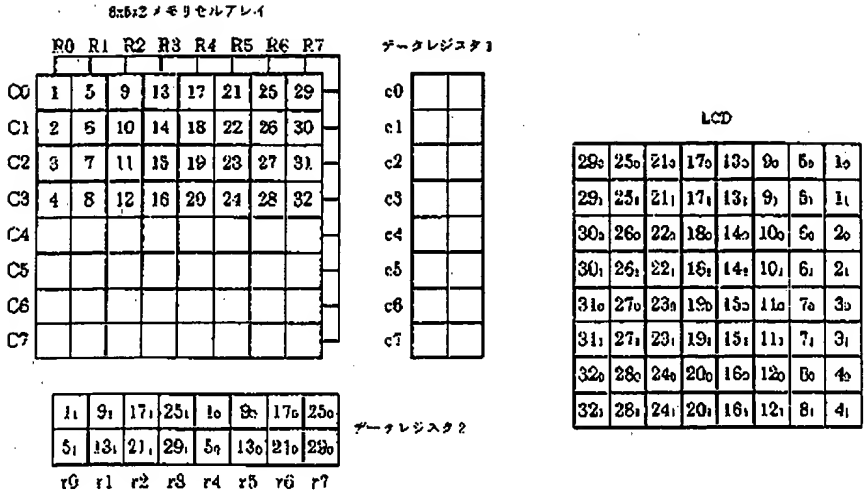
【図10】


8x8x2メモリセルアレイ
R0 R1 R2 R3 R4 R5 R6 R7
C0 1 5 9 13 17 21 25 29
C1 2 6 10 14 18 22 26 30
C2 3 7 11 15 19 23 27 31
C3 4 8 12 16 20 24 28 32
C4
C5
C6
C7
データレジスタ1
c0 29₁ 29₀
c1 30₁ 30₀
c2 31₁ 31₀
c3 32₁ 32₀
c4
c5
c6
c7
r0 r1 r2 r3 r4 r5 r6 r7
データレジスタ2
LCD
32₁ 32₀ 31₁ 31₀ 30₁ 30₀ 29₁ 29₀
28₁ 28₀ 27₁ 27₀ 26₁ 26₀ 25₁ 25₀
24₁ 24₀ 23₁ 23₀ 22₁ 22₀ 21₁ 21₀
20₁ 20₀ 19₁ 19₀ 18₁ 18₀ 17₁ 17₀
16₁ 16₀ 15₁ 15₀ 14₁ 14₀ 13₁ 13₀
12₁ 12₀ 11₁ 11₀ 10₁ 10₀ 9₁ 9₀
8₁ 8₀ 7₁ 7₀ 6₁ 6₀ 5₁ 5₀
4₁ 4₀ 3₁ 3₀ 2₁ 2₀ 1₁ 1₀

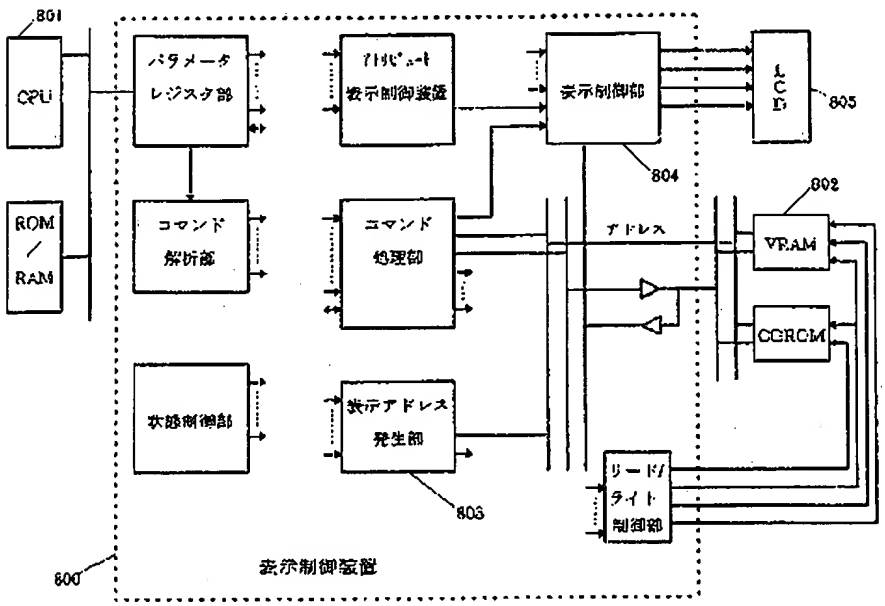
【図11】


8x8x2メモリセルアレイ
R0 R1 R2 R3 R4 R5 R6 R7
C0 1 5 9 13 17 21 25 29
C1 2 6 10 14 18 22 26 30
C2 3 7 11 15 19 23 27 31
C3 4 8 12 16 20 24 28 32
C4
C5
C6
C7
データレジスタ1
c0
c1
c2
c3
c4
c5
c6
c7
4₁ 12₁ 20₁ 28₁ 4₀ 12₀ 20₀ 28₀
8₁ 16₁ 24₁ 32₁ 8₀ 16₀ 24₀ 32₀
データレジスタ2
r0 r1 r2 r3 r4 r5 r6 r7
LCD
4₁ 8₁ 12₁ 16₁ 20₁ 24₁ 28₁ 32₁
4₀ 8₀ 12₀ 16₀ 20₀ 24₀ 28₀ 32₀
3₁ 7₁ 11₁ 15₁ 19₁ 23₁ 27₁ 31₁
3₀ 7₀ 11₀ 15₀ 19₀ 23₀ 27₀ 31₀
2₁ 6₁ 10₁ 14₁ 18₁ 22₁ 26₁ 30₁
2₀ 6₀ 10₀ 14₀ 18₀ 22₀ 26₀ 30₀
1₁ 5₁ 9₁ 13₁ 17₁ 21₁ 25₁ 29₁
1₀ 5₀ 9₀ 13₀ 17₀ 21₀ 25₀ 29₀

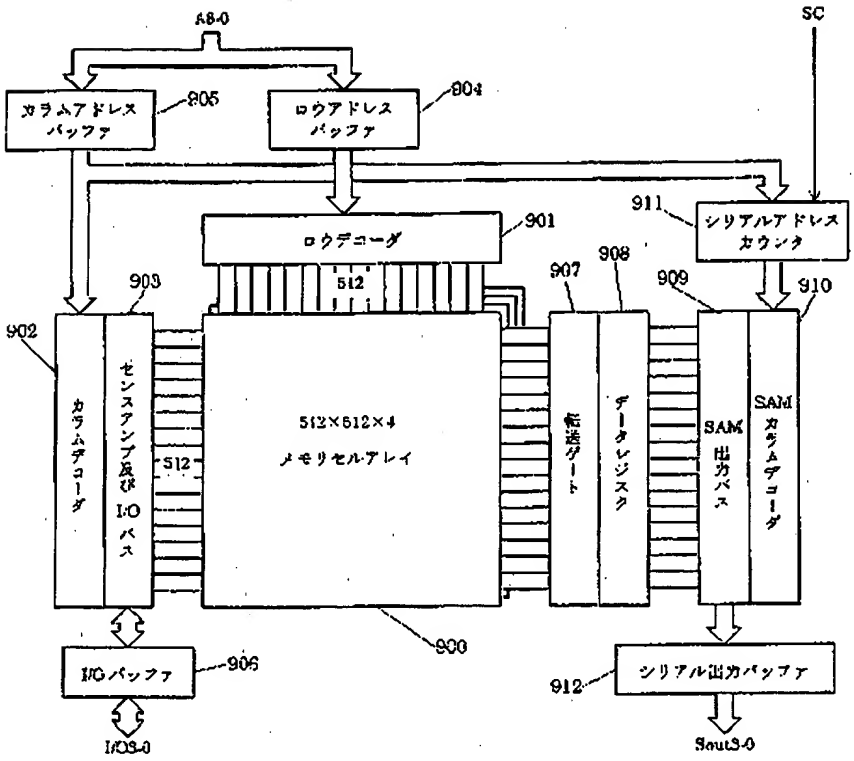
【図12】


8x8x2メモリセルアレイ
R0 R1 R2 R3 R4 R5 R6 R7
C0 1 5 9 13 17 21 25 29
C1 2 6 10 14 18 22 26 30
C2 3 7 11 15 19 23 27 31
C3 4 8 12 16 20 24 28 32
C4
C5
C6
C7
データレジスタ1
c0
c1
c2
c3
c4
c5
c6
c7
LCD
データレジスタ2
r0 r1 r2 r3 r4 r5 r6 r7

【図13】


801
CPU
ROM / RAM
パラメータレジスタ部
コマンド解析部
状態制御部
プリビュー表示制御装置
コマンド処理部
表示アドレス発生部
803
表示制御部
804
LCD
805
アドレス
802
VRAM
CGROM
リード/ライト制御部
600
表示制御装置

【図14】


A8-0
SC
カラムアドレスバッファ
905
ロウアドレスバッファ
904
ロウデコーダ
901
911
シリアルアドレスカウンタ
903
512
907
908
909
910
902
カラムデコーダ
センスアンプ及びI/Oバス
512
512×512×4
メモリセルアレイ
転送ゲート
データレジスタ
SAM出力バス
SAMカラムデコーダ
900
I/Oバッファ
906
912
シリアル出力バッファ
I/O8-0
Sout8-0

CLAIMS

[Claim(s)]
[Claim 1] The multiport memory characterized by to output the data which are the multiport memory which transmits the data memorized by the random-access-memory section to the serial-access-memory section per row address, and performs data output, formed the row address recorder which specifies two or more row addresses which followed said serial-access-memory section for every column address, and the column-address recorder which specifies two or more continuous column addresses for every row address, and were transmitted to said serial-access-memory section as serial data of the direction of a train, or a line writing direction.
[Claim 2] Said row address recorder and said column address recorder are a multiport memory according to claim 1 characterized by outputting the data to which it had the address counter respectively and said row address or column address was transmitted by said serial-access-memory section in order of arbitration an increment or by carrying out a decrement from the start address as serial data of the direction of a train, or a line writing direction.
[Claim 3] The multiport memory according to claim 2 characterized by performing matrix conversion in case the matrix conversion circuit which replaces a row address and a column address is prepared in said random-access-memory section and data are written in it at said random-access-memory section.
[Claim 4] An indicating equipment and said multiport memory which stores the data displayed on said indicating equipment, The display control which reads data from the serial memory section of said multiport memory synchronizing with the screen scan to said indicating equipment, and performs the display to said indicating equipment, The central processing unit which controls the display control concerned is provided. Said central processing unit The transfer to the serial-access-memory section of said multiport memory from the random-access-memory section The row address of the random-access-memory section is made to perform in the direction which carries out a decrement. Said display control two or more row addresses which said serial-access-memory section followed are made to specify for every column address to said multiport memory -- both Make it address towards carrying out the decrement of the column address of the serial-access-memory section from said start address, and a serial data output is made to perform. The display system equipped with the multiport memory according to claim 1 to 3 characterized by rotating 180 degrees and performing image display to said said display.
[Claim 5] Said matrix conversion is performed at the time of the writing to the random-access-memory section of said multiport memory. The transfer to the serial-access-memory section of said multiport memory from the random-access-memory section Carry out in the direction which carries out the decrement of the row address of the random-access-memory section, and two or

more column addresses which said serial-access-memory section followed are made to specify for every row address. With said display control The display system according to claim 4 characterized by displaying the image which rotated the display to said display 270 degrees by reading the row address of the serial-access-memory section from a start address towards incrementing a decrement and a column address.
[Claim 6] Said matrix conversion is performed at the time of the writing to the random-access-memory section of said multiport memory. The transfer to the serial-access-memory section of said multiport memory from the random-access-memory section It carries out in the direction which increments the row address of the random-access-memory section. Two or more column addresses which said serial-access-memory section followed are made to specify for every row address. From said display control, the row address of the serial-access-memory section by reading towards carrying out the decrement of an increment and the column address from a start address The display system according to claim 4 characterized by the ability to display the image which rotated the display to said display 90 degrees.
[Claim 7] The multiport memory characterized by rotating a data list in case it has the RAM section in which random access is possible, and the SAM section corresponding to each of the row address of said RAM section, and a column address in which two serial accesses are possible and data are stored in the SAM section corresponding to the RAM section column address for the column address data of said RAM section.
[Claim 8] An indicating equipment and said multiport memory which memorizes the data displayed on said indicating equipment, The display control which reads data from said SAM section of said multiport memory synchronizing with the screen scan to said indicating equipment, and performs the display to said indicating equipment, The central processing unit which controls said display control is provided. Said SAM section It has a data register respectively corresponding to the row address of said RAM section to said RAM section, and a column address. By performing a data transfer to the data register of said SAM section corresponding to the row address of said RAM section to said RAM section By said display's usually performing a display and a 180-degree rotation display, and performing a data transfer to the data register of said SAM section corresponding to the column address of said RAM section to said RAM section The display system equipped with the multiport memory according to claim 7 characterized by performing a rotation display 90 degrees and 270 degrees with said indicating equipment.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates especially to the rotation display of an image about the display system equipped with the multiport memory and the multiport memory.
[0002]
[Description of the Prior Art] As shown in JP,6-289848,A at drawing 13 , when it has the display address generation section 803 which controls the address of VRAM802 in a display control 800 and a rotation display is directed from CPU801, the change of the generation method of the display address by the display address generation section 803 and a display in the condition that the contents of VRAM802 rotated 180 degrees by the bit rectification of the indicative data

based on a display and control section 804 enabled conventionally, and a high-speed rotation display has realized compared with the method which rewrites by software.
[0003] The multiport RAM shown in drawing 14 Moreover, 4-bit input/output port I/O 3-0 for random access, 4-bit output port Sout 3-0 for serial accesses, and the memory cell array 900 for data storage (512x512x4), The row address decoder 901 which generates the line address of this memory cell array 900, The column address decoder 902 which generates the train address, and the data register 908 which incorporates data per 1 low (row) from the memory cell array 900 through the transfer gate 907, It has the SAM section column address decoder 910 which specifies the address of the data register 908, the serial address counter 911 which increments the SAM section column address synchronizing with a serial access.
[0004] The memory cell array 900 is equipped with four layers of cel array blocks of 512x512 bit pattern. In this multiport RAM, the serial access to the memory cell array (512x512x4) 900 is performed as follows.
[0005] First, a 9-bit line address is sent to the row address buffer 904, and is supplied to the low decoder 901. And it is chosen and the data (512x4) of the memory cell on a Ta line line are stored in the data register 908 in the four-layer cel array layer of the memory cell array (512x512x4) 900 which is the storage section of SAM through the transfer gate 907 of 4 lamination.
[0006] The data stored in the data register 908 are chosen by the SAM column address decoder 910 by 4 bits, and the selected 4 bits are outputted to serial output port Sout 3-0 through the serial output buffer 912 synchronizing with serial clock signal SC. at this time, the increment of the serial address counter 911 is carried out -- having -- the SAM column address decoder 911 -- four bit data of a next address -- choosing . By this actuation, it makes it possible to read the data of a data register 908 continuously.
[0007]
[Problem(s) to be Solved by the Invention] In order to transmit the data on the row address of the RAM section to the data register of the SAM section, to read data in order of an one direction by the serial access from a display and control section in the multiport memory of these conventional technique and to perform a rotation display although the usual display can be performed at high speed, the data in the condition of having rotated when data were written in the RAM section by CPU must be written in, and a load is large for software performing this processing. Moreover, as JP,6-289848,A shows, when performing a rotation display only by the address generation section and the display and control section in an external display control, even if it can do rotation easily 180 degrees, 90 degrees and 270 rotation displays are difficult.
[0008] Then, this invention improves the above trouble and aims at offering the multiport memory which can perform a rotation display easily, and its display system.
[0009]
[Means for Solving the Problem] The row address decoder which specifies a row address as the RAM section in which random access is possible according to claim 1 of this invention, It has the column address decoder which specifies a column address, and the memory cell array which stores data. The data register which stores the data memorized by said RAM section in the SAM section in which a serial access is possible per row address of said RAM section, The transfer gate which transmits data to the data register of the SAM section from the memory cell array of said RAM section in the first half, The SAM section row address decoder and the SAM section column address decoder which specify the address of said data register, It has two serial address counters which increment the row address and column address of the SAM section with a clock

signal. The above-mentioned technical problem is solved by the configuration which can carry out the serial access of the data of the SAM section data register to the direction of a train, or a line writing direction by performing addressing of the SAM section data register in the continuous multi-line and one train or one line, and continuous two or more trains.
[0010] According to claim 2, in the multiport memory of claim 1, it has an increment and the function which can carry out a decrement from the start address which had counted value specified as the SAM section row address counter and the SAM section column address counter, and the above-mentioned technical problem is solved by the configuration which reads the data of the SAM section data register in order of arbitration.
[0011] According to claim 3, in a multiport memory with the configuration of claim 1 and claim 2, the above-mentioned technical problem is solved by the configuration which makes it possible to have the circuit (address line-train conversion circuit) which changes a row address and a column address to the RAM section in which random access is possible, and to replace arrangement of the data written in in a line-train.
[0012] The multiport memory of claim 3 which stores the data displayed on an indicating equipment and this indicating equipment according to claim 4, The display control which reads data from the SAM section of said multiport memory synchronizing with the screen scan to said indicating equipment, and performs the display to said indicating equipment, Provide the central processing unit which controls this display control, and the transfer to the SAM section of said multiport memory from the RAM section is performed in the direction which carries out the decrement of the RAM section row address. Addressing of the SAM section data register is performed by the continuous SAM section row address of a multi-line and the continuous SAM section column address of one train. By reading data by the serial access method towards carrying out the decrement of the SAM section column address from a start address using two serial access clocks from said display control The above-mentioned technical problem is solved by the configuration which makes it possible to rotate 180 degrees and to perform image display to said display.
[0013] According to claim 5, it sets to the display system of claim 4. In the case of the data writing to the RAM section of the multiport memory of claim 3 Exchange of the RAM section row address and the RAM section column address is performed by the address line-train conversion circuit of said RAM section. The transfer to the SAM section of said multiport memory from the RAM section is performed in the direction which carries out the decrement of the RAM section row address. Addressing of the SAM section data register is performed by the SAM section column address of two or more trains which followed the SAM section row address of one line. Two serial access clocks are used from a display control. The SAM section row address from a start address A decrement, By reading data by the serial access method towards incrementing the SAM section column address, the above-mentioned technical problem is solved by the configuration which makes it possible to rotate 270 degrees clockwise and to perform image display to said display.
[0014] According to claim 6, it sets to the display system of claim 4. In the case of the data writing to the RAM section of the multiport memory of claim 3 Exchange of the RAM section row address and the RAM section column address is performed by the address line-train conversion circuit of said RAM section. The transfer to the SAM section of said multiport memory from the RAM section is performed in the direction which increments the RAM section row address. Addressing of the SAM section data register is performed by the SAM section column address of two or more trains which followed the SAM section row address of one line.

Two serial access clocks are used from a display control. The SAM section row address from a start address An increment, By reading data by the serial access method towards carrying out the decrement of the SAM section column address, the above-mentioned technical problem is solved by the configuration which makes it possible to rotate 90 degrees clockwise and to perform image display to said display.

[0015] The row address decoder which specifies a row address as the RAM section in which random access is possible according to claim 7, It has the column address decoder which specifies a column address, and the memory cell array which stores data. The 1st data register which stores the data memorized by the RAM section in the first half in the SAM section in which a serial access is possible per row address of the RAM section in the first half, The 2nd data register which stores the data memorized by the RAM section in the first half per column address of the RAM section in the first half, The transfer gate which transmits data to the data register of the SAM section from the memory cell array of the RAM section in the first half in the first half, The address decoder which specifies the address of a data register in the first half, and the serial address counter which counts the address with a serial access clock, The above-mentioned technical problem is solved by the configuration which can perform a rotation display easily by having the data register selection circuitry which changes selection of two data registers, and changing the list of the memory cell which the column address of the RAM section points out, and the list of the 2nd data register.

[0016] The multiport memory of claim 7 which stores the data displayed on an indicating equipment and this indicating equipment according to claim 8, The display control which reads data from the SAM section of said multiport memory synchronizing with the screen scan to said indicating equipment, and performs the display to said indicating equipment, By providing the central processing unit which controls this display control, and choosing the 1st SAM section data register corresponding to the RAM section row address by the data register selection circuitry of a multiport memory in the first half In the first half by performing the increment and decrement of a serial address counter with the serial access clock from a display control By performing the usual display of an image, and a 180-degree rotation display, and choosing the 2nd SAM section data register corresponding to the RAM section column address by the data register selection circuitry in the first half The above-mentioned technical problem is solved in the first half by the configuration which makes it possible to perform clockwise 90 degrees and image display rotated 270 degrees by performing the increment and decrement of a serial address counter with the serial access clock from a display control.

[0017]

[Embodiment of the Invention] Below, it explains, referring to drawing about the example of this invention. Drawing 1 is the block diagram of the multiport memory of the 1st, the 2nd, and the 3rd invention. Drawing 2 is the block diagram of the display system which used the multiport of drawing 1 . Drawing 5 , drawing 6 , drawing 7 , and drawing 8 show the display condition of data arrangement of a multiport memory in case a rotation display is performed, and LCD by the display system of drawing 2 , respectively, and they use the multiport memory of 8x8x2, and LCD of 8x8 in order to give explanation easy here. LCD is scanned in order toward the lower right from the upper left of drawing.

[0018] As for the memory cell array in which 100 stores an indicative data, and 101, in drawing 1 , the RAM section row address decoder and 102 are the RAM section column address decoders. 103 is a sense amplifier and an I/O bus, and is connected with a system data bus. 104 is an address line-train conversion circuit, and if 90 degrees and 270 rotation displays are directed

clockwise, it will replace the row address and column address of the RAM section. 115 is the transfer gate and transmits the data directed by the row address decoder 101 from the memory cell array 100 of the RAM section to the SAM section. 110 is a data register, and the indicative data transmitted by the transfer gate 115 is stored, and it outputs data by the serial access. 111 is the SAM section row address decoder, 112 is the SAM section column address decoder, and address directions of the multi-line which followed coincidence, and two or more trains can be performed. 113 is a serial address counter for the SAM section row address, 114 is a serial address counter for the SAM section column address, and the increment and decrement from a start address are made, respectively.

[0019] In drawing 2 , as for a central processing unit and 201, LCD and 203 are the multiport memories of drawing 1 , and a display control and 202 have [200] two serial address clocked into.

[0020] In the display system of drawing 2 , when displaying an image in the usual condition, it becomes data arrangement of the memory of drawing 5 . The address line-train conversion circuit 104 does not function, but data are stored in the memory cell array 100 as shown in drawing 5 . Data are transmitted to a data register 110 in order of R7 from the RAM section row address R0. the serial address clock 1 which shows the data transmitted to the data register 110 when the SAM section row address decoder 111 directed continuously the addresses r0 and r1 of two lines and the SAM section column address decoder 112 directed the address of one train in order of c0 to c3 to drawing 1 -- synchronizing -- every [2-bit] -- it is outputted. The usual display is performed by indicating the data by sequential with a display control 201 at LCD202.

[0021] Where an image is rotated 180 degrees, when displaying, it becomes data arrangement of the memory of drawing 6 . The address line-train conversion circuit 104 does not function, but data are stored in the memory cell array 100 as shown in drawing 8 . Data are transmitted to a data register 110 in order of R0 from the RAM section row address R7. the serial address clock 1 which shows the data transmitted to the data register 110 because the SAM section row address decoder 111 directs continuously the addresses r0 and r1 of two lines and the SAM section column address decoder 112 directs the address of one train in order of c3 to c0 to drawing 1 -- synchronizing -- every [2-bit] -- it is outputted. The display of the image which rotated 180 degrees is performed by indicating the data by sequential with a display control 201 at LCD202.

[0022] Where an image is rotated 270 degrees clockwise, when displaying, it becomes data arrangement of the memory of drawing 7 . The RAM section row address and the RAM section column address are replaced by the address line-train conversion circuit 104, and data are stored in the memory cell array 100 as shown in drawing 7 . Data are transmitted to a data register 110 in order of R0 from the RAM section row address R3. the serial address clock 1 which the data which the SAM section row address r1 directs when the SAM section row address decoder 111 directs the address r1 of one line and the SAM section column address decoder 112 directs the address of two trains in order of c0 and c1 to c6 and c7 show to drawing 1 -- synchronizing -- every [2-bit] -- it is outputted. next, the serial address clock 1 which the data which the SAM section row address r0 directs when directions of the SAM section row address are moved to r0 and the column address decoder 112 directs the address of two trains once again by inputting the serial address clock 2 shown in drawing 1 in order of c0 and c1 to c6 and c7 show to drawing 1 -- synchronizing -- every [2-bit] -- it is outputted. The display of the image which rotated 270 degrees clockwise is performed by indicating the data by sequential with a display control 201 at LCD202.

[0023] Where an image is rotated 90 degrees clockwise, when displaying, it becomes data

arrangement of the memory of drawing 8 . The RAM section row address and the RAM section column address are replaced by the address line-train conversion circuit 104, and data are stored in the memory cell array 100 as shown in drawing 8 . Data are transmitted to a data register 110 in order of R3 from the RAM section row address R0. the serial address clock 1 which the data which the SAM section row address r0 directs when the SAM section row address decoder 111 directs the address r0 of one line and the SAM section column address decoder 112 directs the address of two trains in order of c7 and c6 to c1 and c0 show to drawing 1 -- synchronizing -- every [2-bit] -- it is outputted. next, the serial address clock 1 which the data which the SAM section row address r1 directs when directions of the SAM section row address are moved to r1 and the column address decoder 112 directs the address of two trains once again by inputting the serial address clock 2 shown in drawing 1 in order of c7 and c6 to c1 and c0 show to drawing 1 -- synchronizing -- every [2-bit] -- it is outputted. The display of the image which rotated 90 degrees clockwise is performed by indicating the data by sequential with a display control 201 at LCD202.

[0024] Drawing 3 is the block diagram of the multiport memory of other examples of this invention. Drawing 4 is the block diagram of the display system which used the multiport of drawing 3 . Drawing 9 , drawing 10 , drawing 11 , and drawing 12 show the display condition of data arrangement of a multiport memory in case a rotation display is performed, and LCD by the display system of drawing 4 , respectively, and they use the multiport memory of 8x8x2, and LCD of 8x8 in order to give explanation easy here. LCD is scanned in order toward the lower right from the upper left of drawing.

[0025] As for the memory cell array in which 300 stores an indicative data, and 301, in drawing 3 , the RAM section row address decoder and 302 are the RAM section column address decoders. 303 is connected with a system data bus by the sense amplifier and the I/O bus. 315 transmits the data directed by the row address decoder 301 from the memory cell array 300 of the RAM section at the transfer gate to the SAM section. The indicative data transmitted by the transfer gate 315 with a data register is stored, and 310 outputs data by the serial access. 325 is the transfer gate and the data directed by the column address decoder 302 from the memory cell array 300 of the RAM section are transmitted to the SAM section. 320 is arranged so that a rotation display may be easily performed in the indicative data transmitted by the transfer gate 325 with a data register, and it outputs data by the serial access. 312 is an address decoder for a data register 310, and 322 is an address decoder for a data register 320. 314 is a serial address counter for the SAM section address decoders 312 and 322, and can do the increment and decrement from a start address, respectively. It is a data register selection circuitry which [of two data registers 310 and 320] 330 uses, and for choosing.

[0026] For 400, as for a display control and 402, in drawing 4 , a central processing unit and 401 are [LCD and 403] the multiport memories of drawing 3 . In the display system of drawing 4 , when displaying an image in the usual condition, it becomes data arrangement of the memory of drawing 9 . Data are stored in the memory cell array 300 as shown in drawing 9 . A data register 310 is chosen by the data register selection circuitry 330, and data are transmitted to a data register 310 in order of R7 from the RAM section row address R0. the data transmitted to the data register 310 when the SAM section address decoder 312 directed the address in order of c0 to c3 -- a serial address clock -- synchronizing -- every [2-bit] -- it is outputted. The usual display is performed by indicating the data by sequential with a display control 401 at LCD402.

[0027] Where an image is rotated 180 degrees, when displaying, it becomes data arrangement of the memory of drawing 10 . Data are stored in the memory cell array 300 as shown in drawing

10 . A data register 310 is chosen by the data register selection circuitry 330, and data are transmitted to a data register 310 in order of R0 from the RAM section row address R7. the data transmitted to the data register 310 when the SAM section address decoder 312 directed the address in order of c3 to c0 -- a serial address clock -- synchronizing -- every [2-bit] -- it is outputted. The display of the image which rotated 180 degrees is performed by indicating the data by sequential with a display control 401 at LCD402.

[0028] Where an image is rotated 270 degrees clockwise, when displaying, it becomes data arrangement of the memory of drawing 11 . Data are stored in the memory cell array 300 as shown in drawing 11 . A data register 320 is chosen by the data register selection circuitry 330, and data are transmitted to a data register 320 in order of C0 from the RAM section column address C3. The data transmitted to the data register 320 are arranged as shown in drawing 11 . the data transmitted to the data register 320 when the SAM section address decoder 322 directed the address in order of r0 to r7 -- a serial address clock -- synchronizing -- every [2-bit] -- it is outputted. The display of the image which rotated 270 degrees clockwise is performed by indicating the data by sequential with a display control 401 at LCD402.

[0029] Where an image is rotated 90 degrees clockwise, when displaying, it becomes data arrangement of the memory of drawing 12 . Data are stored in the memory cell array 300 as shown in drawing 12 . A data register 320 is chosen by the data register selection circuitry 330, and data are transmitted to a data register 320 in order of C3 from the RAM section column address C0. The data transmitted to the data register 320 are arranged as shown in drawing 12 . the data transmitted to the data register 320 when the SAM section address decoder 322 directed the address in order of r7 to r0 -- a serial address clock -- synchronizing -- every [2-bit] -- it is outputted. The display of the image which rotated 90 degrees clockwise is performed by indicating the data by sequential with a display control 401 at LCD402.

[0030]

[Effect of the Invention] Since the row address recorder which specifies two or more row addresses which followed the serial-access-memory section for every column address, and the column address recorder which specifies two or more continuous column addresses for every row address were formed according to the multiport memory according to claim 1 and rotation processing of an image can be performed within a multiport memory, it is effective in a high-speed rotation display being attained compared with the method which rewrites the contents of the multiport memory by software.

[0031] According to the multiport memory according to claim 2, in a multiport memory according to claim 1, it is effective in the ability to output an increment or the data transmitted to said serial-access-memory section in order of arbitration as serial data of the direction of a train, or a line writing direction from a start address, since a decrement is carried out in said row address or column address.

[0032] Since according to the multiport memory according to claim 3 matrix conversion is performed in a multiport memory according to claim 2 in case data are written in said random-access-memory section, in case data are written in the random-access-memory section, it is effective in the ability to perform matrix conversion automatically.

[0033] According to the display system according to claim 4 to 6, it is effective in it becoming unnecessary to write the data based on software etc. which carried out rotation processing in a multiport memory, and being able to realize a very high-speed rotation display by the multiport memory according to claim 1 to 3, in case the image is indicated by rotation 270 degrees 180 degrees 90 degrees.

[0034] Since according to the multiport memory according to claim 7 a data list is rotated in case data are stored in the SAM section corresponding to the RAM section column address for the column address data of the RAM section, it is effective in the ability to change a data list required for a rotation display easily.
[0035] According to the multiport memory according to claim 8, it sets to a multiport memory according to claim 7. By performing a data transfer to the data register of said SAM section corresponding to the row address of said RAM section to said RAM section By said display's usually performing a display and a 180-degree rotation display, and performing a data transfer to the data register of said SAM section corresponding to the column address of said RAM section to said RAM section Since said display performs a rotation display 90 degrees and 270 degrees, it becomes unnecessary to write the data based on software etc. which carried out rotation processing in a multiport memory, and is effective in a very high-speed rotation display being realizable.

TECHNICAL FIELD

[Field of the Invention] This invention relates especially to the rotation display of an image about the display system equipped with the multiport memory and the multiport memory.

PRIOR ART

[Description of the Prior Art] As shown in JP,6-289848,A at drawing 13 , when it has the display address generation section 803 which controls the address of VRAM802 in a display control 800 and a rotation display is directed from CPU801, the change of the generation method of the display address by the display address generation section 803 and a display in the condition that the contents of VRAM802 rotated 180 degrees by the bit rectification of the indicative data based on a display and control section 804 enabled conventionally, and a high-speed rotation display has realized compared with the method which rewrites by software.
[0003] The multiport RAM shown in drawing 14 Moreover, 4-bit input/output port I/O 3-0 for random access, 4-bit output port Sout 3-0 for serial accesses, and the memory cell array 900 for data storage (512x512x4), The row address decoder 901 which generates the line address of this memory cell array 900, The column address decoder 902 which generates the train address, and the data register 908 which incorporates data per 1 low (row) from the memory cell array 900 through the transfer gate 907, It has the SAM section column address decoder 910 which specifies the address of the data register 908, the serial address counter 911 which increments the SAM section column address synchronizing with a serial access.
[0004] The memory cell array 900 is equipped with four layers of cel array blocks of 512x512 bit pattern. In this multiport RAM, the serial access to the memory cell array (512x512x4) 900 is performed as follows.
[0005] First, a 9-bit line address is sent to the row address buffer 904, and is supplied to the low decoder 901. And it is chosen and the data (512x4) of the memory cell on a Ta line line are stored in the data register 908 in the four-layer cel array layer of the memory cell array (512x512x4) 900 which is the storage section of SAM through the transfer gate 907 of 4

lamination.
[0006] The data stored in the data register 908 are chosen by the SAM column address decoder 910 by 4 bits, and the selected 4 bits are outputted to serial output port Sout 3-0 through the serial output buffer 912 synchronizing with serial clock signal SC. at this time, the increment of the serial address counter 911 is carried out -- having -- the SAM column address decoder 911 -- four bit data of a next address -- choosing . By this actuation, it makes it possible to read the data of a data register 908 continuously.

EFFECT OF THE INVENTION

[Effect of the Invention] Since the row address recorder which specifies two or more row addresses which followed the serial-access-memory section for every column address, and the column address recorder which specifies two or more continuous column addresses for every row address were formed according to the multiport memory according to claim 1 and rotation processing of an image can be performed within a multiport memory, it is effective in a high-speed rotation display being attained compared with the method which rewrites the contents of the multiport memory by software.
[0031] According to the multiport memory according to claim 2, in a multiport memory according to claim 1, it is effective in the ability to output an increment or the data transmitted to said serial-access-memory section in order of arbitration as serial data of the direction of a train, or a line writing direction from a start address, since a decrement is carried out in said row address or column address.
[0032] Since according to the multiport memory according to claim 3 matrix conversion is performed in a multiport memory according to claim 2 in case data are written in said random-access-memory section, in case data are written in the random-access-memory section, it is effective in the ability to perform matrix conversion automatically.
[0033] According to the display system according to claim 4 to 6, it is effective in it becoming unnecessary to write the data based on software etc. which carried out rotation processing in a multiport memory, and being able to realize a very high-speed rotation display by the multiport memory according to claim 1 to 3, in case the image is indicated by rotation 270 degrees 180 degrees 90 degrees.
[0034] Since according to the multiport memory according to claim 7 a data list is rotated in case data are stored in the SAM section corresponding to the RAM section column address for the column address data of the RAM section, it is effective in the ability to change a data list required for a rotation display easily.
[0035] According to the multiport memory according to claim 8, in a multiport memory according to claim 7, a data transfer is performed to the data register of said SAM section corresponding to the row address of said RAM section to said RAM section, Since said display performs a rotation display 90 degrees and 270 degrees by said display's usually performing a display and a 180-degree rotation display, and performing a data transfer to the data register of said SAM section corresponding to the column address of said RAM section to said RAM section, it becomes unnecessary to write the data based on software etc. which carried out rotation processing in a multiport memory, and is effective in a very high-speed rotation display being realizable.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] In order to transmit the data on the row address of the RAM section to the data register of the SAM section, to read data in order of an one direction by the serial access from a display and control section in the multiport memory of these conventional technique and to perform a rotation display although the usual display can be performed at high speed, the data in the condition of having rotated when data were written in the RAM section by CPU must be written in, and a load is large for software performing this processing. Moreover, as JP,6-289848,A shows, when performing a rotation display only by the address generation section and the display and control section in an external display control, even if it can do rotation easily 180 degrees, 90 degrees and 270 rotation displays are difficult.
[0008] Then, this invention improves the above trouble and aims at offering the multiport memory which can perform a rotation display easily, and its display system.

MEANS

[Means for Solving the Problem] The row address decoder which specifies a row address as the RAM section in which random access is possible according to claim 1 of this invention, It has the column address decoder which specifies a column address, and the memory cell array which stores data. The data register which stores the data memorized by said RAM section in the SAM section in which a serial access is possible per row address of said RAM section, The transfer gate which transmits data to the data register of the SAM section from the memory cell array of said RAM section in the first half, The SAM section row address decoder and the SAM section column address decoder which specify the address of said data register, It has two serial address counters which increment the row address and column address of the SAM section with a clock signal. The above-mentioned technical problem is solved by the configuration which can carry out the serial access of the data of the SAM section data register to the direction of a train, or a line writing direction by performing addressing of the SAM section data register in the continuous multi-line and one train or one line, and continuous two or more trains.
[0010] According to claim 2, in the multiport memory of claim 1, it has an increment and the function which can carry out a decrement from the start address which had counted value specified as the SAM section row address counter and the SAM section column address counter, and the above-mentioned technical problem is solved by the configuration which reads the data of the SAM section data register in order of arbitration.
[0011] According to claim 3, in a multiport memory with the configuration of claim 1 and claim 2, the above-mentioned technical problem is solved by the configuration which makes it possible to have the circuit (address line-train conversion circuit) which changes a row address and a column address to the RAM section in which random access is possible, and to replace arrangement of the data written in in a line-train.
[0012] The multiport memory of claim 3 which stores the data displayed on an indicating equipment and this indicating equipment according to claim 4, The display control which reads data from the SAM section of said multiport memory synchronizing with the screen scan to said indicating equipment, and performs the display to said indicating equipment, Provide the central

processing unit which controls this display control, and the transfer to the SAM section of said multiport memory from the RAM section is performed in the direction which carries out the decrement of the RAM section row address. Addressing of the SAM section data register is performed by the continuous SAM section row address of a multi-line and the continuous SAM section column address of one train. By reading data by the serial access method towards carrying out the decrement of the SAM section column address from a start address using two serial access clocks from said display control The above-mentioned technical problem is solved by the configuration which makes it possible to rotate 180 degrees and to perform image display to said display.

[0013] According to claim 5, it sets to the display system of claim 4. In the case of the data writing to the RAM section of the multiport memory of claim 3 Exchange of the RAM section row address and the RAM section column address is performed by the address line-train conversion circuit of said RAM section. The transfer to the SAM section of said multiport memory from the RAM section is performed in the direction which carries out the decrement of the RAM section row address. Addressing of the SAM section data register is performed by the SAM section column address of two or more trains which followed the SAM section row address of one line. Two serial access clocks are used from a display control. The SAM section row address from a start address A decrement, By reading data by the serial access method towards incrementing the SAM section column address, the above-mentioned technical problem is solved by the configuration which makes it possible to rotate 270 degrees clockwise and to perform image display to said display.

[0014] According to claim 6, it sets to the display system of claim 4. In the case of the data writing to the RAM section of the multiport memory of claim 3 Exchange of the RAM section row address and the RAM section column address is performed by the address line-train conversion circuit of said RAM section. The transfer to the SAM section of said multiport memory from the RAM section is performed in the direction which increments the RAM section row address. Addressing of the SAM section data register is performed by the SAM section column address of two or more trains which followed the SAM section row address of one line. Two serial access clocks are used from a display control. The SAM section row address from a start address An increment, By reading data by the serial access method towards carrying out the decrement of the SAM section column address, the above-mentioned technical problem is solved by the configuration which makes it possible to rotate 90 degrees clockwise and to perform image display to said display.

[0015] The row address decoder which specifies a row address as the RAM section in which random access is possible according to claim 7, It has the column address decoder which specifies a column address, and the memory cell array which stores data. The 1st data register which stores the data memorized by the RAM section in the first half in the SAM section in which a serial access is possible per row address of the RAM section in the first half, The 2nd data register which stores the data memorized by the RAM section in the first half per column address of the RAM section in the first half, The transfer gate which transmits data to the data register of the SAM section from the memory cell array of the RAM section in the first half in the first half, The address decoder which specifies the address of a data register in the first half, and the serial address counter which counts the address with a serial access clock, The above-mentioned technical problem is solved by the configuration which can perform a rotation display easily by having the data register selection circuitry which changes selection of two data registers, and changing the list of the memory cell which the column address of the RAM section

points out, and the list of the 2nd data register.
[0016] The multiport memory of claim 7 which stores the data displayed on an indicating equipment and this indicating equipment according to claim 8, The display control which reads data from the SAM section of said multiport memory synchronizing with the screen scan to said indicating equipment, and performs the display to said indicating equipment, By providing the central processing unit which controls this display control, and choosing the 1st SAM section data register corresponding to the RAM section row address by the data register selection circuitry of a multiport memory in the first half In the first half by performing the increment and decrement of a serial address counter with the serial access clock from a display control By performing the usual display of an image, and a 180-degree rotation display, and choosing the 2nd SAM section data register corresponding to the RAM section column address by the data register selection circuitry in the first half The above-mentioned technical problem is solved in the first half by the configuration which makes it possible to perform clockwise 90 degrees and image display rotated 270 degrees by performing the increment and decrement of a serial address counter with the serial access clock from a display control.
[0017]
[Embodiment of the Invention] Below, it explains, referring to drawing about the example of this invention. Drawing 1 is the block diagram of the multiport memory of the 1st, the 2nd, and the 3rd invention. Drawing 2 is the block diagram of the display system which used the multiport of drawing 1 . Drawing 5 , drawing 6 , drawing 7 , and drawing 8 show the display condition of data arrangement of a multiport memory in case a rotation display is performed, and LCD by the display system of drawing 2 , respectively, and they use the multiport memory of 8x8x2, and LCD of 8x8 in order to give explanation easy here. LCD is scanned in order toward the lower right from the upper left of drawing.
[0018] As for the memory cell array in which 100 stores an indicative data, and 101, in drawing 1 , the RAM section row address decoder and 102 are the RAM section column address decoders. 103 is a sense amplifier and an I/O bus, and is connected with a system data bus. 104 is an address line-train conversion circuit, and if 90 degrees and 270 rotation displays are directed clockwise, it will replace the row address and column address of the RAM section. 115 is the transfer gate and transmits the data directed by the row address decoder 101 from the memory cell array 100 of the RAM section to the SAM section. 110 is a data register, and the indicative data transmitted by the transfer gate 115 is stored, and it outputs data by the serial access. 111 is the SAM section row address decoder, 112 is the SAM section column address decoder, and address directions of the multi-line which followed coincidence, and two or more trains can be performed. 113 is a serial address counter for the SAM section row address, 114 is a serial address counter for the SAM section column address, and the increment and decrement from a start address are made, respectively.
[0019] In drawing 2 , as for a central processing unit and 201, LCD and 203 are the multiport memories of drawing 1 , and a display control and 202 have [200] two serial address clocked into.
[0020] In the display system of drawing 2 , when displaying an image in the usual condition, it becomes data arrangement of the memory of drawing 5 . The address line-train conversion circuit 104 does not function, but data are stored in the memory cell array 100 as shown in drawing 5 . Data are transmitted to a data register 110 in order of R7 from the RAM section row address R0. the serial address clock 1 which shows the data transmitted to the data register 110 when the SAM section row address decoder 111 directed continuously the addresses r0 and r1 of

two lines and the SAM section column address decoder 112 directed the address of one train in order of c0 to c3 to drawing 1 -- synchronizing -- every [2-bit] -- it is outputted. The usual display is performed by indicating the data by sequential with a display control 201 at LCD202.
[0021] Where an image is rotated 180 degrees, when displaying, it becomes data arrangement of the memory of drawing 6 . The address line-train conversion circuit 104 does not function, but data are stored in the memory cell array 100 as shown in drawing 8 . Data are transmitted to a data register 110 in order of R0 from the RAM section row address R7. the serial address clock 1 which shows the data transmitted to the data register 110 because the SAM section row address decoder 111 directs continuously the addresses r0 and r1 of two lines and the SAM section column address decoder 112 directs the address of one train in order of c3 to c0 to drawing 1 -- synchronizing -- every [2-bit] -- it is outputted. The display of the image which rotated 180 degrees is performed by indicating the data by sequential with a display control 201 at LCD202.
[0022] Where an image is rotated 270 degrees clockwise, when displaying, it becomes data arrangement of the memory of drawing 7 . The RAM section row address and the RAM section column address are replaced by the address line-train conversion circuit 104, and data are stored in the memory cell array 100 as shown in drawing 7 . Data are transmitted to a data register 110 in order of R0 from the RAM section row address R3. the serial address clock 1 which the data which the SAM section row address r1 directs when the SAM section row address decoder 111 directs the address r1 of one line and the SAM section column address decoder 112 directs the address of two trains in order of c0 and c1 to c6 and c7 show to drawing 1 -- synchronizing -- every [2-bit] -- it is outputted. next, the serial address clock 1 which the data which the SAM section row address r0 directs when directions of the SAM section row address are moved to r0 and the column address decoder 112 directs the address of two trains once again by inputting the serial address clock 2 shown in drawing 1 in order of c0 and c1 to c6 and c7 show to drawing 1 -- synchronizing -- every [2-bit] -- it is outputted. The display of the image which rotated 270 degrees clockwise is performed by indicating the data by sequential with a display control 201 at LCD202.
[0023] Where an image is rotated 90 degrees clockwise, when displaying, it becomes data arrangement of the memory of drawing 8 . The RAM section row address and the RAM section column address are replaced by the address line-train conversion circuit 104, and data are stored in the memory cell array 100 as shown in drawing 8 . Data are transmitted to a data register 110 in order of R3 from the RAM section row address R0. the serial address clock 1 which the data which the SAM section row address r0 directs when the SAM section row address decoder 111 directs the address r0 of one line and the SAM section column address decoder 112 directs the address of two trains in order of c7 and c6 to c1 and c0 show to drawing 1 -- synchronizing -- every [2-bit] -- it is outputted. next, the serial address clock 1 which the data which the SAM section row address r1 directs when directions of the SAM section row address are moved to r1 and the column address decoder 112 directs the address of two trains once again by inputting the serial address clock 2 shown in drawing 1 in order of c7 and c6 to c1 and c0 show to drawing 1 -- synchronizing -- every [2-bit] -- it is outputted. The display of the image which rotated 90 degrees clockwise is performed by indicating the data by sequential with a display control 201 at LCD202.
[0024] Drawing 3 is the block diagram of the multiport memory of other examples of this invention. Drawing 4 is the block diagram of the display system which used the multiport of drawing 3 . Drawing 9 , drawing 10 , drawing 11 , and drawing 12 show the display condition of data arrangement of a multiport memory in case a rotation display is performed, and LCD by the

display system of drawing 4 , respectively, and they use the multiport memory of 8x8x2, and LCD of 8x8 in order to give explanation easy here. LCD is scanned in order toward the lower right from the upper left of drawing.

[0025] As for the memory cell array in which 300 stores an indicative data, and 301, in drawing 3 , the RAM section row address decoder and 302 are the RAM section column address decoders. 303 is connected with a system data bus by the sense amplifier and the I/O bus. 315 transmits the data directed by the row address decoder 301 from the memory cell array 300 of the RAM section at the transfer gate to the SAM section. The indicative data transmitted by the transfer gate 315 with a data register is stored, and 310 outputs data by the serial access. 325 is the transfer gate and the data directed by the column address decoder 302 from the memory cell array 300 of the RAM section are transmitted to the SAM section. 320 is arranged so that a rotation display may be easily performed in the indicative data transmitted by the transfer gate 325 with a data register, and it outputs data by the serial access. 312 is an address decoder for a data register 310, and 322 is an address decoder for a data register 320. 314 is a serial address counter for the SAM section address decoders 312 and 322, and can do the increment and decrement from a start address, respectively. It is a data register selection circuitry which [of two data registers 310 and 320] 330 uses, and for choosing.

[0026] For 400, as for a display control and 402, in drawing 4 , a central processing unit and 401 are [LCD and 403] the multiport memories of drawing 3 . In the display system of drawing 4 , when displaying an image in the usual condition, it becomes data arrangement of the memory of drawing 9 . Data are stored in the memory cell array 300 as shown in drawing 9 . A data register 310 is chosen by the data register selection circuitry 330, and data are transmitted to a data register 310 in order of R7 from the RAM section row address R0. the data transmitted to the data register 310 when the SAM section address decoder 312 directed the address in order of c0 to c3 -- a serial address clock -- synchronizing -- every [2-bit] -- it is outputted. The usual display is performed by indicating the data by sequential with a display control 401 at LCD402.

[0027] Where an image is rotated 180 degrees, when displaying, it becomes data arrangement of the memory of drawing 10 . Data are stored in the memory cell array 300 as shown in drawing 10 . A data register 310 is chosen by the data register selection circuitry 330, and data are transmitted to a data register 310 in order of R0 from the RAM section row address R7. the data transmitted to the data register 310 when the SAM section address decoder 312 directed the address in order of c3 to c0 -- a serial address clock -- synchronizing -- every [2-bit] -- it is outputted. The display of the image which rotated 180 degrees is performed by indicating the data by sequential with a display control 401 at LCD402.

[0028] Where an image is rotated 270 degrees clockwise, when displaying, it becomes data arrangement of the memory of drawing 11 . Data are stored in the memory cell array 300 as shown in drawing 11 . A data register 320 is chosen by the data register selection circuitry 330, and data are transmitted to a data register 320 in order of C0 from the RAM section column address C3. The data transmitted to the data register 320 are arranged as shown in drawing 11 . the data transmitted to the data register 320 when the SAM section address decoder 322 directed the address in order of r0 to r7 -- a serial address clock -- synchronizing -- every [2-bit] -- it is outputted. The display of the image which rotated 270 degrees clockwise is performed by indicating the data by sequential with a display control 401 at LCD402.

[0029] Where an image is rotated 90 degrees clockwise, when displaying, it becomes data arrangement of the memory of drawing 12 . Data are stored in the memory cell array 300 as shown in drawing 12 . A data register 320 is chosen by the data register selection circuitry 330,

and data are transmitted to a data register 320 in order of C3 from the RAM section column address C0. The data transmitted to the data register 320 are arranged as shown in drawing 12 . the data transmitted to the data register 320 when the SAM section address decoder 322 directed the address in order of r7 to r0 -- a serial address clock -- synchronizing -- every [2-bit] -- it is outputted. The display of the image which rotated 90 degrees clockwise is performed by indicating the data by sequential with a display control 401 at LCD402.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram of the multiport memory of the gestalt of 1 operation of this invention.
[Drawing 2] It is the block diagram of the gestalt display system of 1 operation of this invention.
[Drawing 3] It is the block diagram of the multiport memory of the gestalt of other operations of this invention.
[Drawing 4] It is the block diagram of the display system of the gestalt of other operations of this invention.
[Drawing 5] It is the data plot plan of the multiport memory at the time of the usual display in the display system of drawing 2 .
[Drawing 6] It is the data plot plan of the multiport memory at the time of the 180-degree rotation display in the display system of drawing 2 .
[Drawing 7] It is the data plot plan of the multiport memory at the time of a 270-degree rotation display at the clockwise rotation in the display system of drawing 2 .
[Drawing 8] It is the data plot plan of the multiport memory at the time of a 90-degree rotation display at the clockwise rotation in the display system of drawing 2 .
[Drawing 9] It is the data plot plan of the multiport memory at the time of the usual display in the display system of drawing 4 .
[Drawing 10] It is the data plot plan of the multiport memory at the time of the 180-degree rotation display in the display system of drawing 4 .
[Drawing 11] It is the data plot plan of the multiport memory at the time of a 270-degree rotation display at the clockwise rotation in the display system of drawing 4 .
[Drawing 12] It is the data plot plan of the multiport memory at the time of a 90-degree rotation display at the clockwise rotation in the display system of drawing 4 .
[Drawing 13] It is the block diagram of a basing-on conventional technique display system.
[Drawing 14] It is the block diagram of the multiport memory by the conventional technique.
[Description of Notations]
100 Memory Cell Array
101 The RAM Section Row Address Decoder
102 The RAM Section Column Address Decoder
103 Sense Amplifier and I/O Bus
104 Address Line-Train Conversion Circuit
110 Data Register
111 The SAM Section Row Address Decoder
112 The SAM Section Column Address Decoder
113 Serial Address Counter 2

114 Serial Address Counter 1
115 Transfer Gate
200 Central Processing Unit
201 Display Control
202 LCD
203 Multiport Memory
300 Memory Cell Array
301 The RAM Section Row Address Decoder
302 The RAM Section Column Address Decoder
303 Sense Amplifier and I/O Bus
310 Data Register 1
312 The SAM Section Address Decoder 1
314 Serial Address Counter
315 Transfer Gate 1
320 Data Register 2
322 The SAM Section Address Decoder 2
325 Transfer Gate 2
330 Data Register Selection Circuitry
400 Central Processing Unit
401 Display Control
402 LCD
403 Multiport Memory
800 Display Control
801 CPU
802 VRAM
803 Display Address Generation Section
804 Display and Control Section
805 LCD
900 Memory Cell Array
901 The RAM Section Low Decoder
902 The RAM Section Column Decoder
903 Sense Amplifier and I/O Bus
904 Row Address Buffer
905 Column Address Buffer
906 I/O Buffer
907 Transfer Gate
908 Data Register
909 The SAM Section Output Bus
910 The SAM Section Column Decoder
911 Serial Address Counter
912 Serial Output Buffer